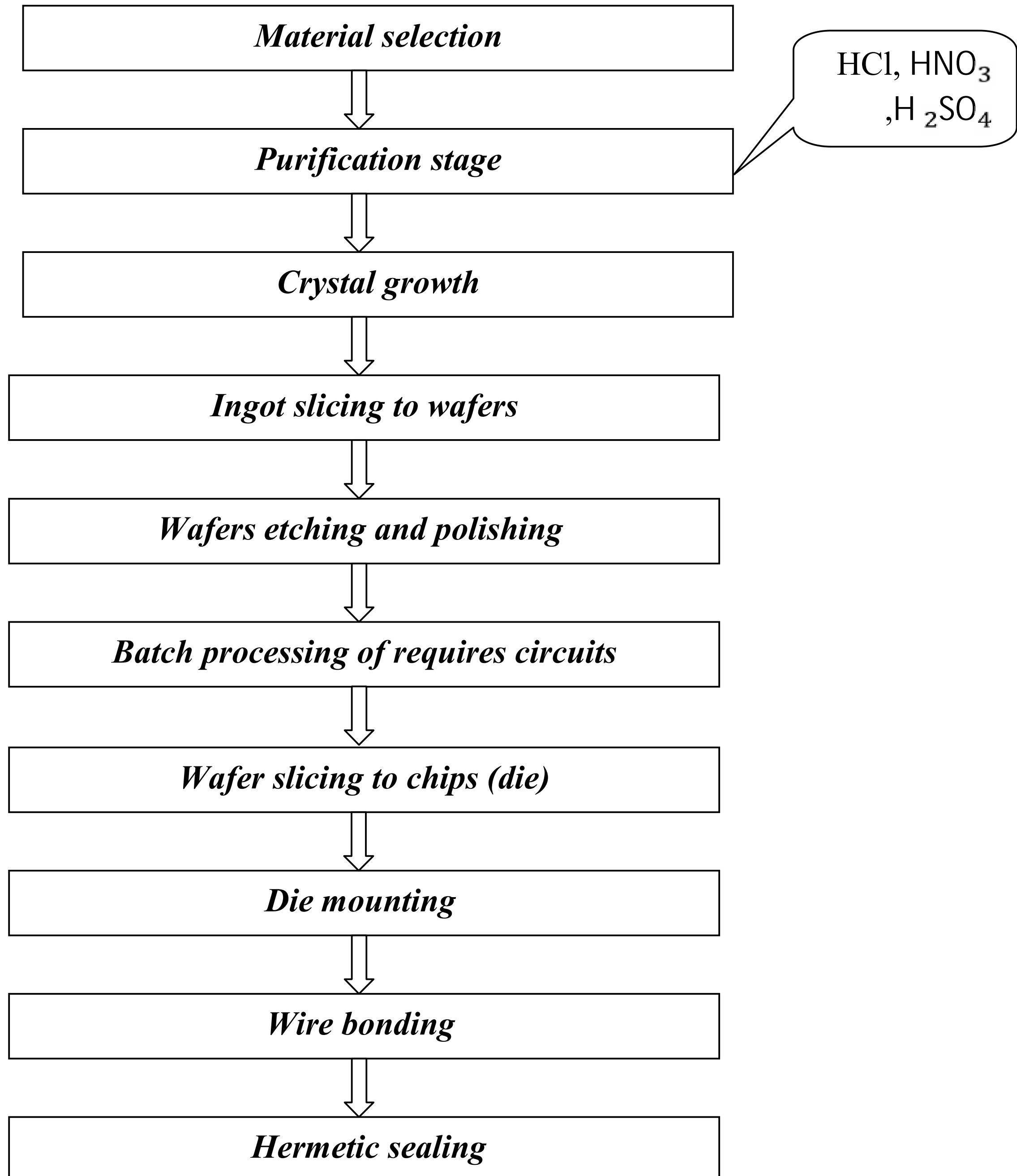
Lecture number: Two

Title : IC fabrication

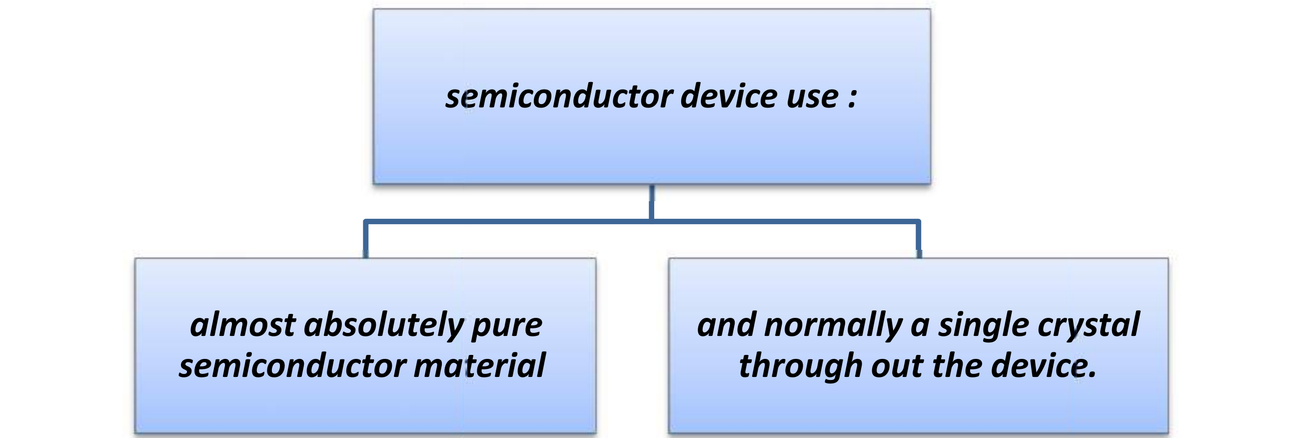
The development of semiconductors technology



1)Material selection

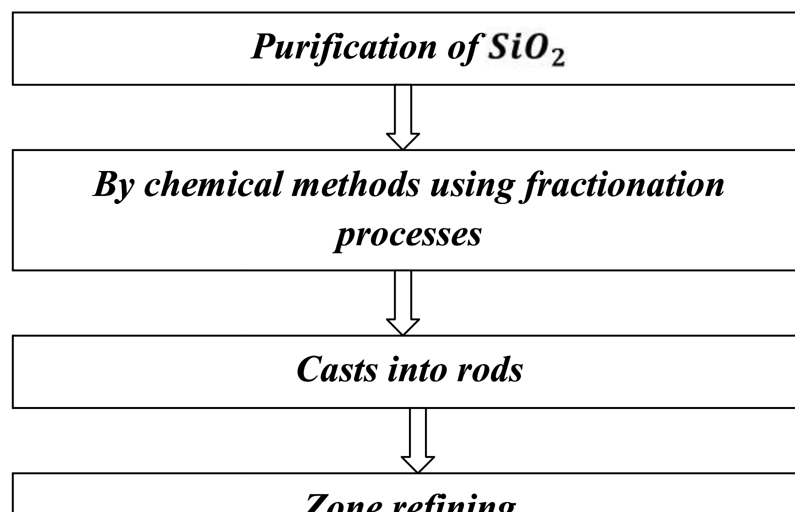
Since most monolithic integrated circuits are now fabricated in silicon, our discussion will be limited to preparation os substrates made from this semiconductor. The most commonly occurring natural sources of silicon are its oxides ,e,g., sand and quartz. These can be reduced in a furnace with carbon to

produce 98 per cent pure silicon. However, this impurity level is much too high for semiconductor device preparation; atypical requirement might be for less than one impurity atom per10^9 silicon for the starting material, so the commercial silicon requires considerable refining before it is suitable. So to design semiconductor device use: *almost absolutely pure semiconductor material and normally a single crystal through out the device.*



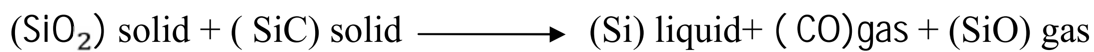
2) ***Purification stage:***

The most commonly occurring natural sources of silicon are silica and silicates .At present silicon made devices constitute over 95% of all semiconductor devices. Where silicon is always found in natural in a compound form such as sand and quartz (SiO_2).The sand used to grow the wafers has to be a very clean and good form of silicon . For this reason not just any sand scraped off the beach will do. Most of the sand used for these processes is shipped from the beaches of Australia. Where the main steps of purification are :



The raw material of single crystal silicon is the electronic grade silicon(EGS) which is a polycrystalline material of high purity .the major impurity in the EGS are boron ,carbon, and residual donor. Pure EGS should have doping elements in the part of billion range ,and carbon less than 2 parts per million . production of EGS is multi steps as shown in figure ().

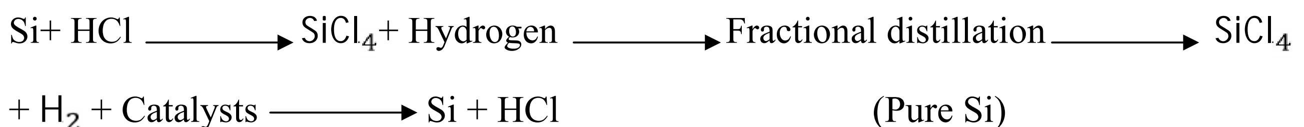
First ,a metallurgical grade silicon(MGS) is produce in an arc furnace which is charged with quartzite, a relatively pure form of sand (SiO_2).,and carbon in the form of coal, coke, and wood chips. The over all reaction in the furnace being



(SiO_2) solid + (SiC) solid ⟶ (Si) liquid+ (CO)gas + (SiO) gas

These can be reduced in a furnace with carbon to produce 98 per cent pure silicon. However, this impurity level is much too high for semiconductor device preparation: atypical requirement might be for less than one atom per 10^9 silicon atom for the starting material, so the commercial silicon requires considerable refining before it is suitable.

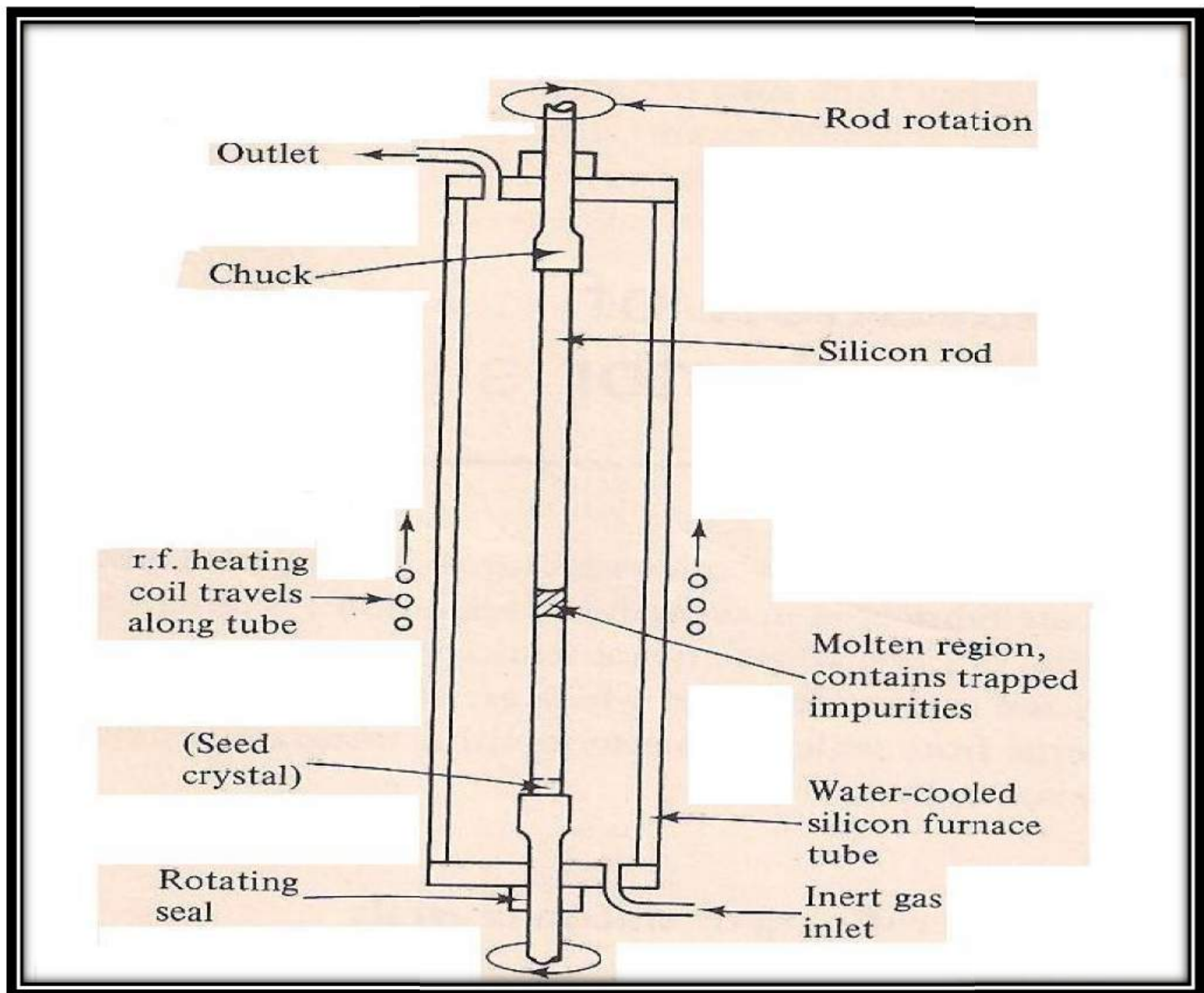
Quartzite(SiO_2) +Carbon(C)+Heat(about 1600 degrees C)+ catalysts ⟶ Si+ CO_2 (Raw Si)



Si+ HCl ⟶ $SiCl_4$+ Hydrogen ⟶ Fractional distillation ⟶ $SiCl_4$ + H_2 + Catalysts ⟶ Si + HCl (Pure Si)

One technique used for the purification of industrial silicon is known as zone refining. The apparatus used is shown in schematically in figure(1). The silicon is cast into along , thin ingot which is selectively heated locally, usually by an induction heating coil, to produce a short molten section. The molten silicon is prevented from separating from the ingot by surface_tension forces. Since most

impurity atoms in silicon have an affinity for liquid rather than the solid state ,they are trapped in the narrow molten zone; hence, if the heating coil is slowly traversed the rod ,taking the molten region with it, the impurities are confined to this region and are swept to one end of the bar. After several such passes , unwanted impurities are almost entirely concentrated at the ends of the bar, which can be subsequently cut off and discarded.



Figure(1) Schematic diagram of zone _refining equipment

٣) Crystal growth:

There are several methods to grow a single crystal of semiconductor such as :

1. Czochralski method.
2. Epitaxial growth :from gas phase on a single crystal substrate.

-LPE:Liquid Phase Epitaxial.

-VPE:Vapor Phase Epitaxial.

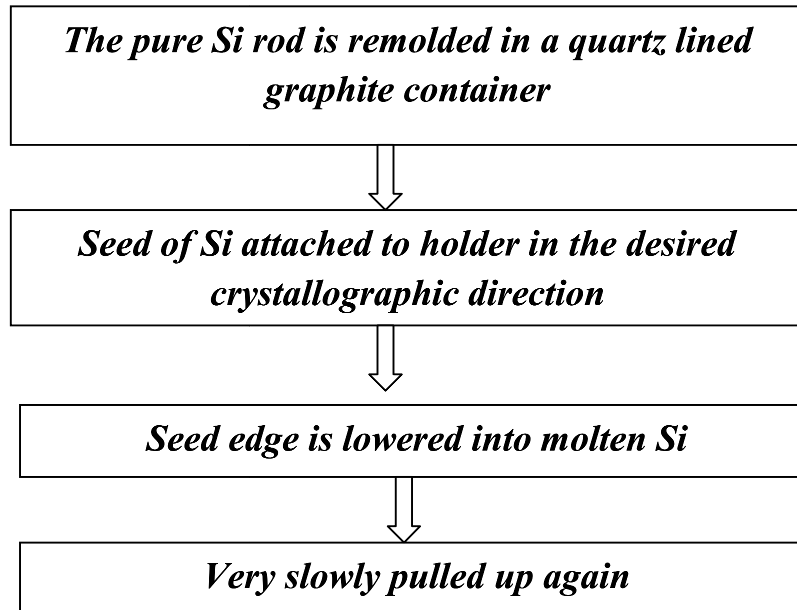
-MBE:Molecular Beam Epitaxial.

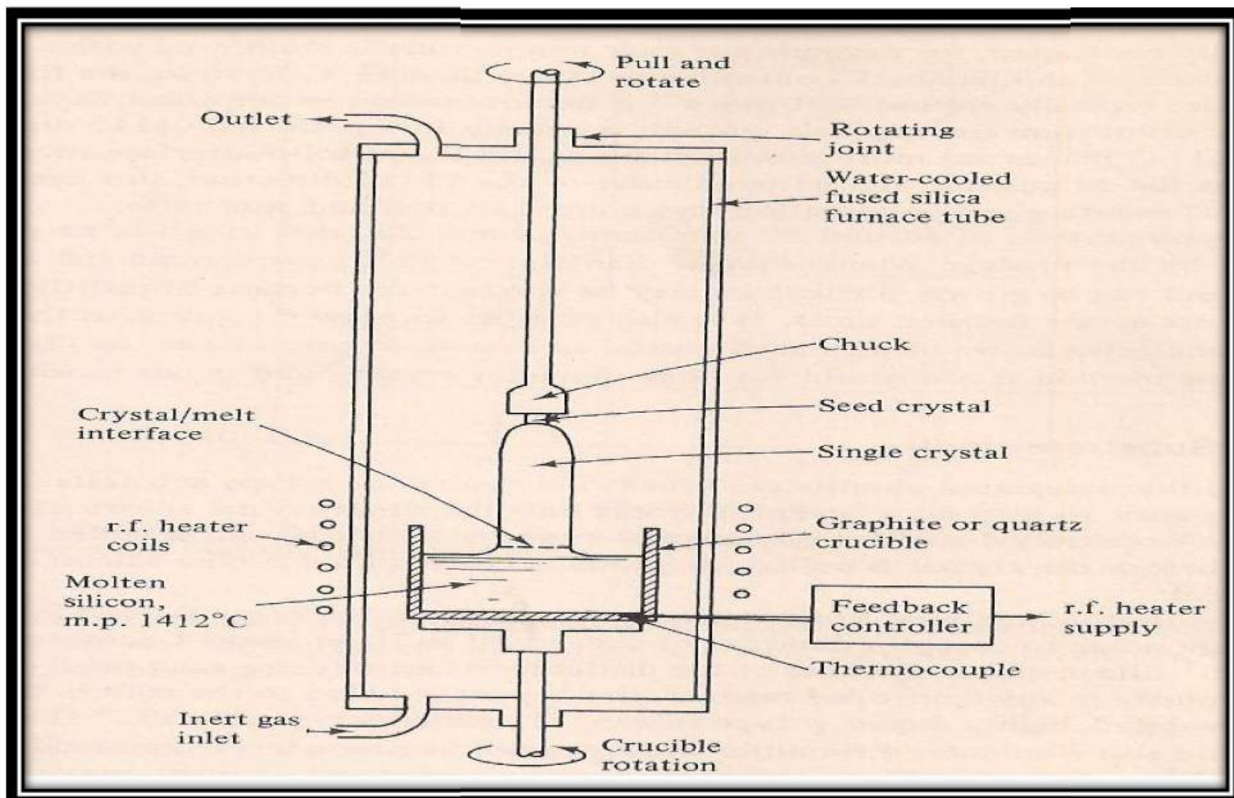
3. Metal Organic CVD (MOCVD).
4. CVD (Chemical Vapor Deposition)
5. Plasma deposition.

The most common one is the : "Czochralski pulling method"; Although the silicon is at this stage highly refined and free from impurities it is still polycrystalline, and a necessary requirement for substrates is that it is single crystal semiconductor. A difficulty is that the concentration of atoms in the molten material is very much greater than in the regular diamond lattice of the crystalline form; this precludes methods of crystal growth in crucibles, which would result in material containing many dislocations.

A procedure for growing silicon crystals which has found wide commercial use, the Czochralski method, obviates this difficulty. A correctly oriented seed crystal is partly immersed in molten refined silicon. The melt temperature is then reduced slightly until silicon begins to freeze on the cooler seed crystal. Which is then slowly withdrawn. See figure(2). If the temperature and withdrawal rate are correctly chosen, the liquid –solid interface remains near to the surface of the melt and along signal-crystal of silicon is pulled from it. This process is also carried out in an inter atmosphere, probably argon or helium, to prevent oxidation. A further refinement is that both melt and puller are continuously rotated, to produce a more homogeneous crystal. The result is a pure silicon cylinder that is called an ingot. Monolithic integrated circuits are usually fabricated on P_type substrates, so it is necessary to introduce acceptor atoms into the single crystal silicon at some stage . A controlled amount of acceptor impurity, often boron, is added to the melt before the crystal is pulled, to produce the required p_type silicon substrate material. When the ingot is the correct length, it is removed, then ground to a uniform external surface and

diameter. Each of the wafers is given either a notch or a flat edge that will be used later in orienting the wafer into the exact position for later procedures.. The main Czochralski method. steps are:





Figure(2) schematic diagram of apparatus of single_ crystal silicon by the czochralski method

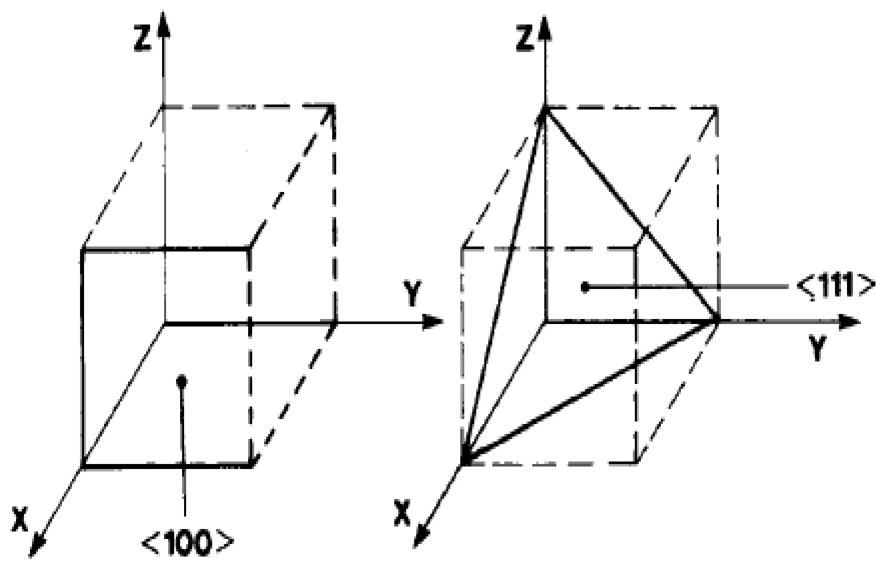


Figure 3.6 Crystal planes.

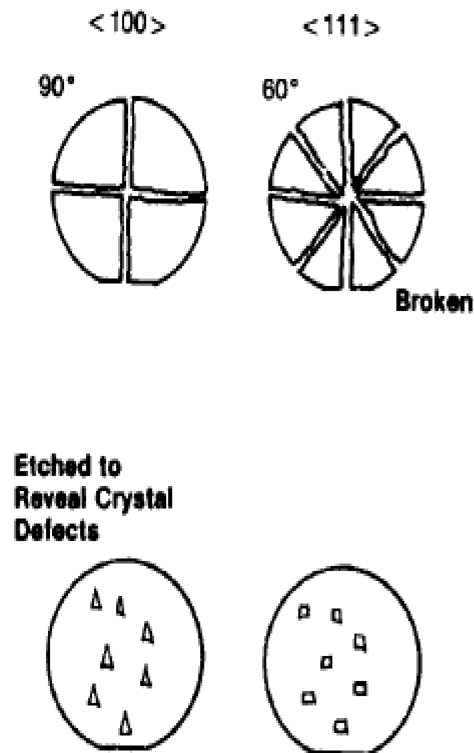


Figure 3.7 Wafer orientation indicators.

into quarters or with right angle (90°) breaks. The ⟨111⟩ wafers break into triangular pieces.

EPITAXY

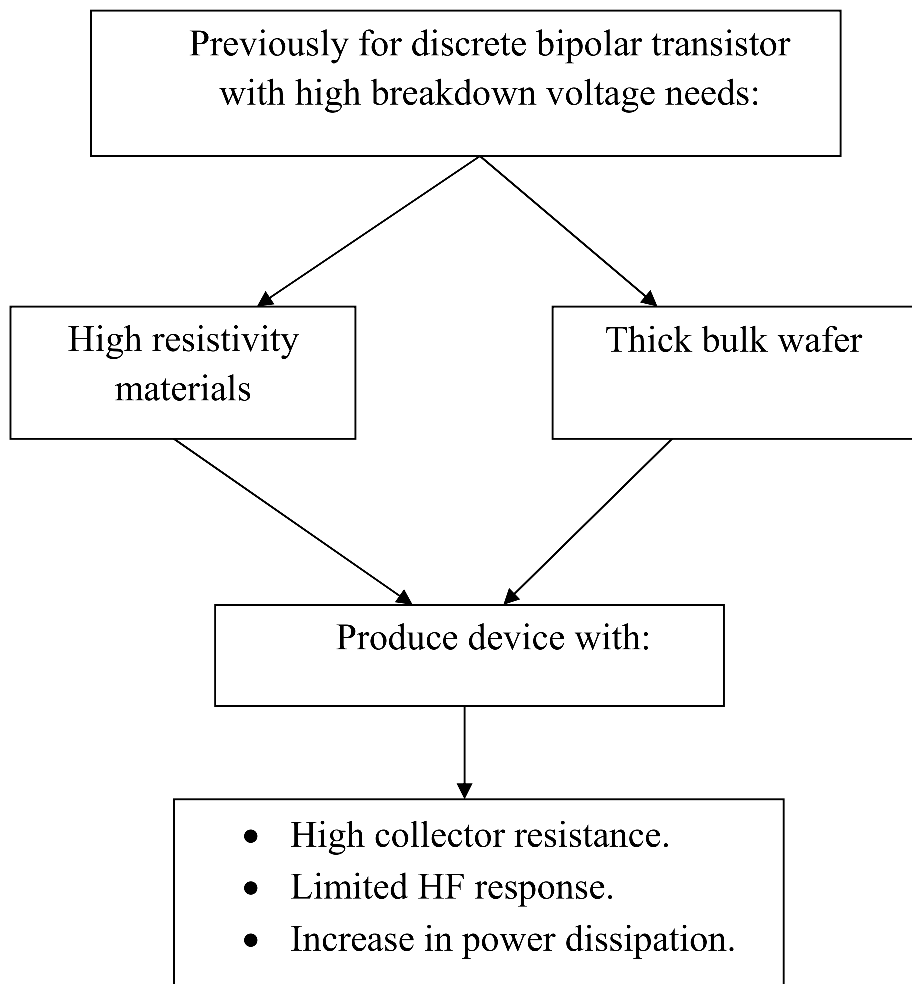
EPI TAXI

Greek word mean upon ***Greek word mean ordered***

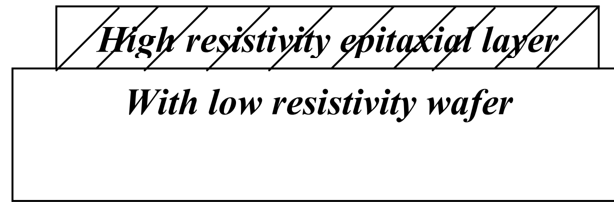
EPITAXY: it is a process used to growth a thin crystalline layer of material upon a single crystal substrate, such as (Si), so that the lattice structure of the layer is identical to the substrate.

Why epitaxial growth is used ?

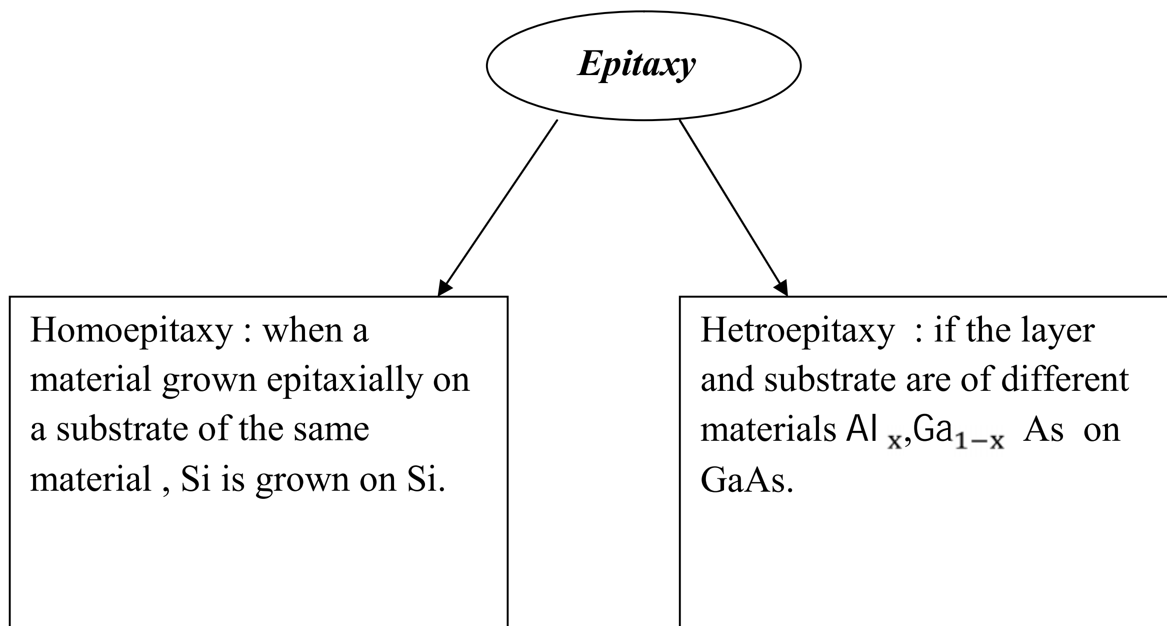
1) Bulk _grown crystals of sufficiently good, for direct fabrication are difficult to grow.



Now with epitaxial growth we get high resistivity epitaxial layer with low resistivity wafer.



2) Epitaxial structures improve the performance of dynamic RAM devices and CMOS ICs.
3) The epitaxial layer on a substrate (often) contain one or more buried layers which offers the designer means of controlling the doping profile in a device structure beyond that available with diffusion or ion implantation.
4) The physical property of epitaxial layer differs from the bulk material (free from O_2 and C).
5) High quality devices.
6) Easy to control the impurity concentrations.



Epitaxial methods

1) VPE: Vapor Phase Epitaxial.
2) MBE: Molecular Beam Epitaxial.
3) LPE: Liquid Phase Epitaxial.

Vapor phase growth

This is technique is employed in semiconductor technology for the deposition of :

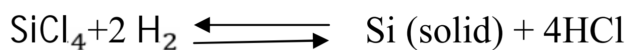
1) Metal (Aluminum).
2) Insulators (SiO_2).
3) Semiconductors (Si).

This technique is very important for the growth of (epitaxial) layers.

Epitaxial growth: means the growth of a single crystal semiconductor film upon a single crystal substrate of the same semiconductor. it's important is due to :

1) The ease of controlling the impurity concentration in the film in dependently of the impurities within the substrate by controlling their concentration in the gas.
2) It can be used to grow film of low impurity concentration upon substrates of higher impurity concentration.

Epitaxial layer preparation : there are several ways to prepare epitaxial growth, but the common one is the : ***vapor phase reduction of silicon tetrachloride.***



$$SiCl_4 + 2H_2 \rightleftharpoons Si\ (solid) + 4HCl$$

- ❖ Silicon tetrachloride vapor carried in a stream of hydrogen gas is passed through the furnace.
- ❖ The silicon is deposition and forms a single crystal on the substrate surface.
- ❖ The crystal can be deliberately doped n-type and p-type by fistly bubbling the hydrogen through a weak solution of: phosphorous tri chloride (n-type) or boron tri chloride (p-type).
- ❖ Epitaxial layers of thickness 2-20 *M*m can be produced.

Another VPE system for GaAs and InP, consider GaAs growth:

- Ga is used as the source material and held at 200 C^0.
- Crust must form over the entire surface before crystal growth begins to ensure arsenic saturation.
- Back etch (dissolving) is carried out by running the system at relatively high temperature of (850- 900) C^0.
- Epitaxial layer is deposited at (710-750) C^0.
- Highly doped material may be grown by moving the material up stream and lightly doped by moving it downstream in the (H_2S) gas.
- By balancing the arsenic chloride $AsCl_3$flow relative to H_2 flow, it is possible to control the ambient net donor density over a significant range.

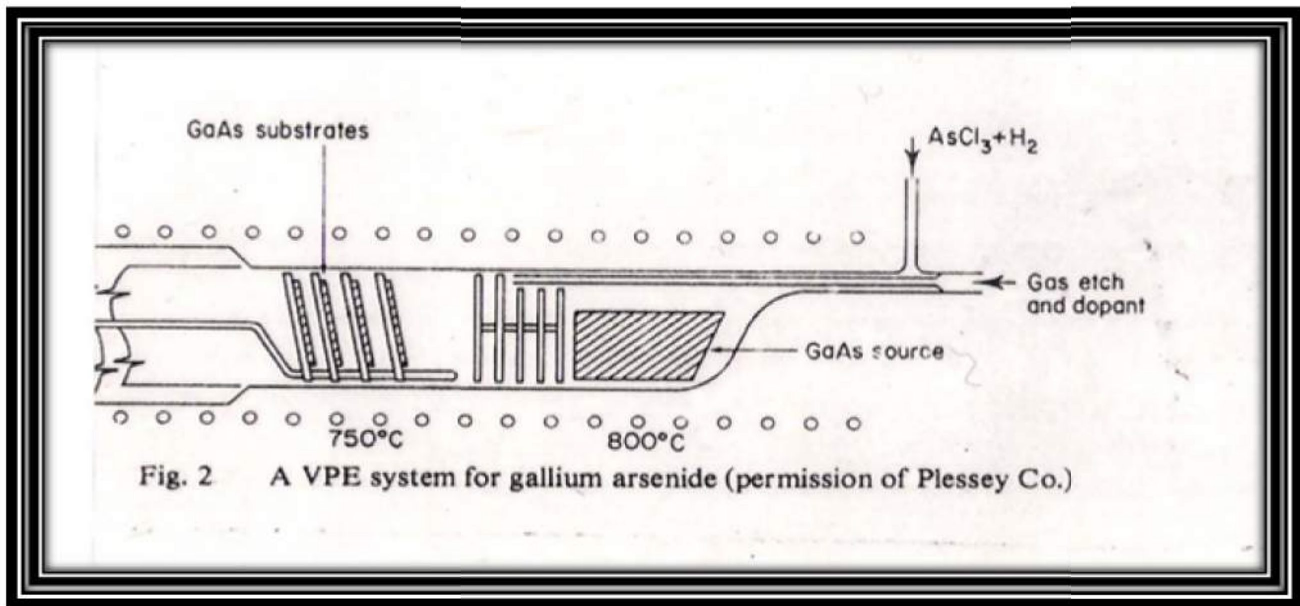
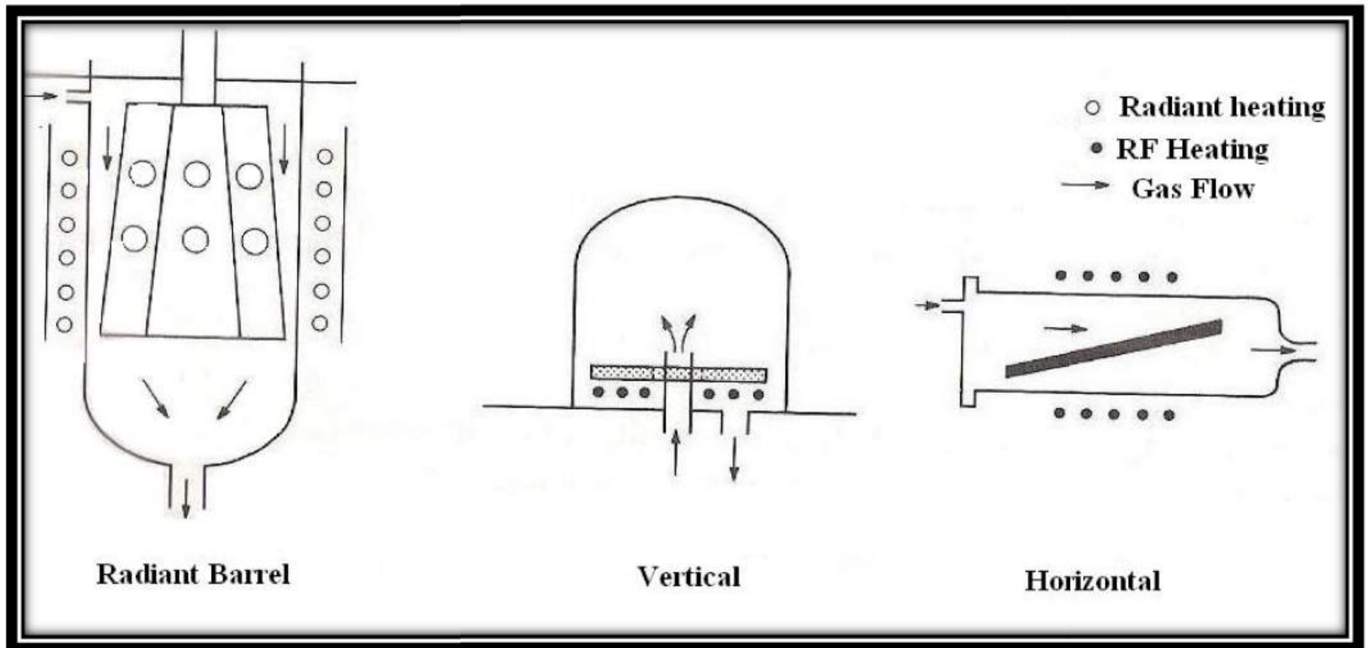


Fig. 2 A VPE system for gallium arsenide (permission of Plessey Co.)

<u>Epitaxial growth reactors :</u>

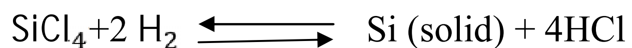
There are three basic reactors configurations:

1) Horizontal.
2) Pancake or vertical.
3) Barrel.



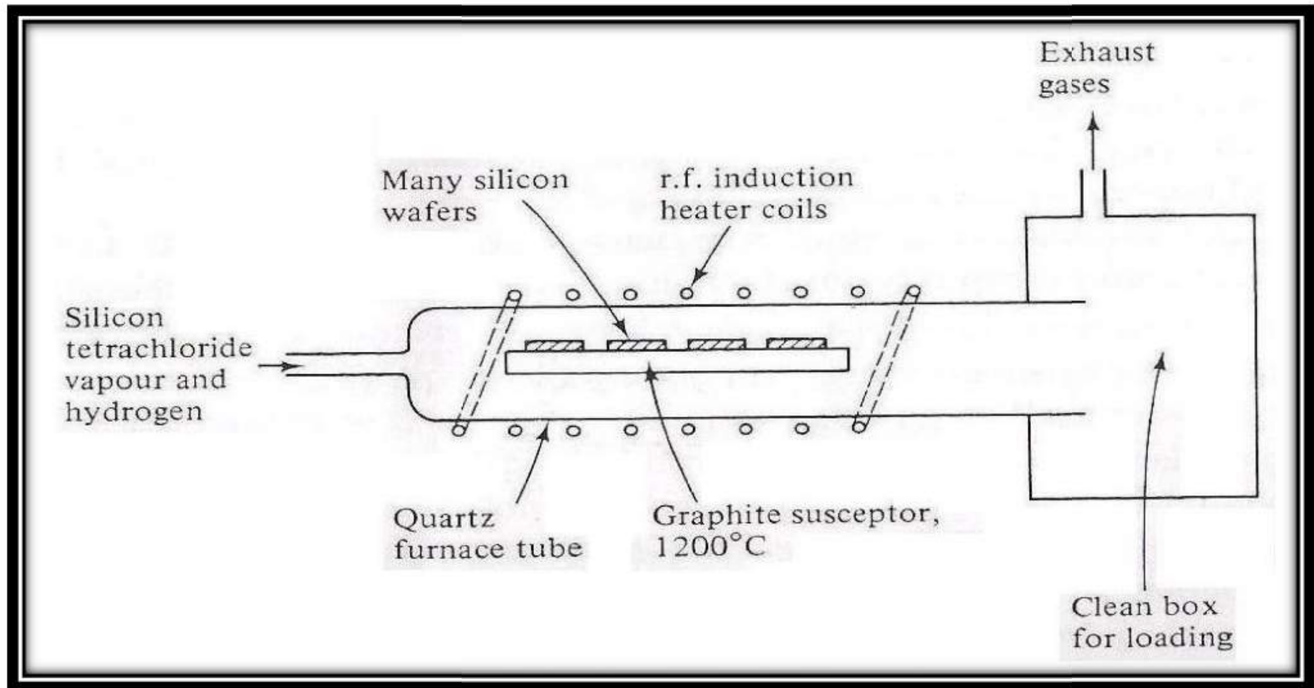
reactors configuration

In the vapor phase technique, silicon chloride vapor is reduced with hydrogen on the surface of silicon substrate slices, which are heated in an r. f. induction furnace, to produce silicon indirectly:



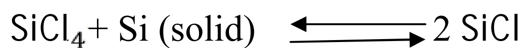
$$SiCl_4 + 2H_2 \rightleftharpoons Si\ (solid) + 4HCl$$

The schematic diagram of horizontal reactor is shown in figure below with some details.



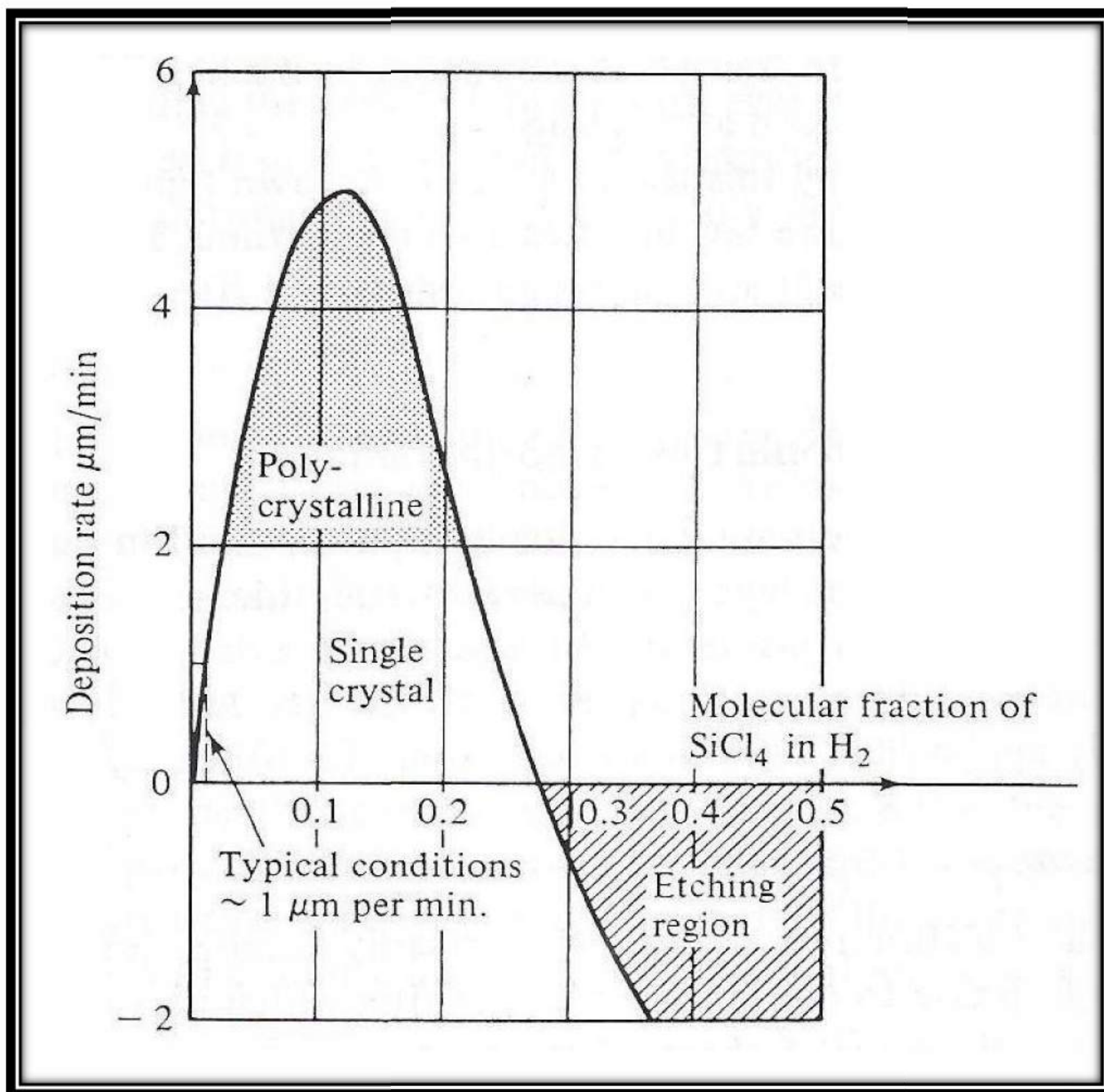
Horizontal reactor for epitaxial silicon layer growth

The temperature of reactor is kept, typically, at 1200C°. if the temperature of the reactor is reduced much below this value , the epi _layers become more defective and eventually noncrystalline, because of the reduce mobility of the deposit atoms and their subsequent difficulty in moving to correct sites in the crystal lattice. Note that if the chemical reaction indicated by the equation is reversible. Hence, if hydrogen chloride vapor is present in the carrier gas, etching rather than epitaxial growth occurs. When the concentration of silicon tetrachloride is high, etching can still occur even when hydrogen chloride is not present, due to a competing interaction.



$$SiCl_4 + Si\ (solid) \rightleftharpoons 2\ SiCl$$

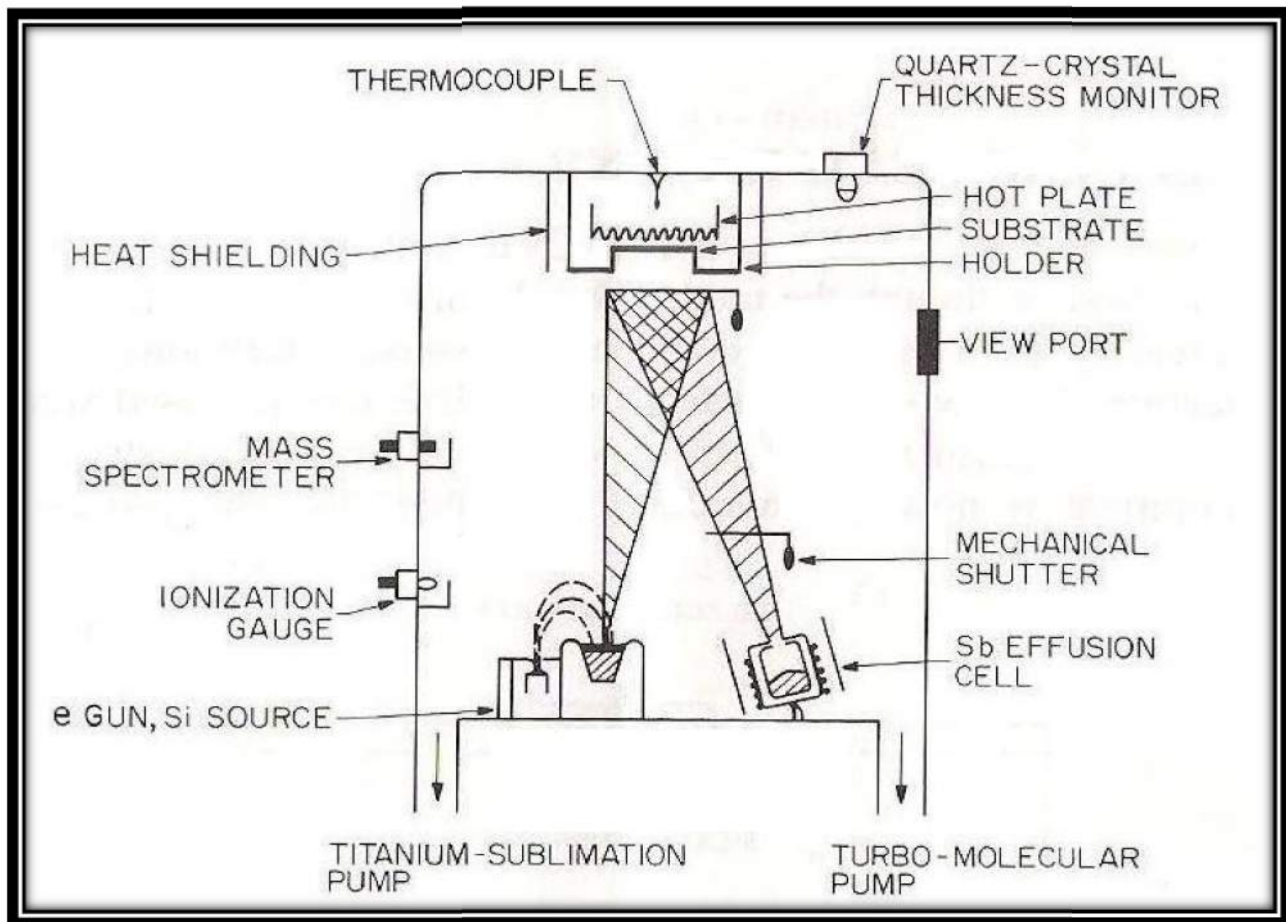
Thus the growth rate of epitaxial silicon, which will be negative if etching occurs, is very critically dependent on the concentration of silicon chloride as well as the temperature , as shown in figure below . it will be note that the typical industrial conditions for growth at a rate of around 1 Mm per minute produce layers which are well within the region for single crystal epitaxy.



The variation of growth /etching rate with concentration of silicon chloride, at some particular temperature

Molecular Beam Epitaxial

The basis of this technique is to allow abeam of the desired constituent atoms to fall upon, and stick to, a desired substrate held at elevated temperature in ultra high vacuum chosen such that it allows the best quality crystal to grow on the substrate.



Schematic of MBE growth system

Why MBE were not used widely although it is know since 1960?

1) The film quality was not commensurate with a device needs.
2) No industrial equipment existed.

advantages of MBE (over CVD)?

1) Low temperature processing, this will reduce the outdiffusion and autodoping.
2) The precise control of doping.
3) MBE is not complicated by boundary _layer transport effects nor are there chemical reactions to consider.

Present applications :

1) Discrete microwave devices (varactors, diodes used as FM modulators).
2) Photonic devices.

MBE process:

- Evaporation of Si and one more dopants.
- These species are transported at relatively high velocity in vacuum to the substrate.
- The low vapor pressure of Si and the dopants ensure condensation on a low temperature substrate.
- The usual pressure p =10^{-8} to 10^{-10} Torr.

-The mean free path of the atoms is (L = 5 * 10^{-3} / P) Where L is the mean free path in Cm , and P is the pressure in Torr . At a system pressure of 10^{-9} , L would be 5 * 10^{6} Cm.

-temperature range 400-800 C °.

-growth rate : 0.01 -0.3 *M*m/min.

- pre cleaning of MBE is done by :
    1. High temperature baking between 1000-1250 C °for up to 30 minutes. This decomposes (the native oxide, adsorbed species (notably carbon)).
    2. By using low _energy beam of an inter gas to sputter clean the surface. A short anneal at 800-900 C ° is sufficient to reorder the surface.

Liquid Phase Epitaxial

-The substrate (seed) crystal is held above a semiconductor melt and then dipped into it.

-as the substrate is withdrawn from the melt to the cooler region of the furnace the molten film covering the surface will form an epitaxial crystalline layer provided the rate of cooling is carefully controlled.

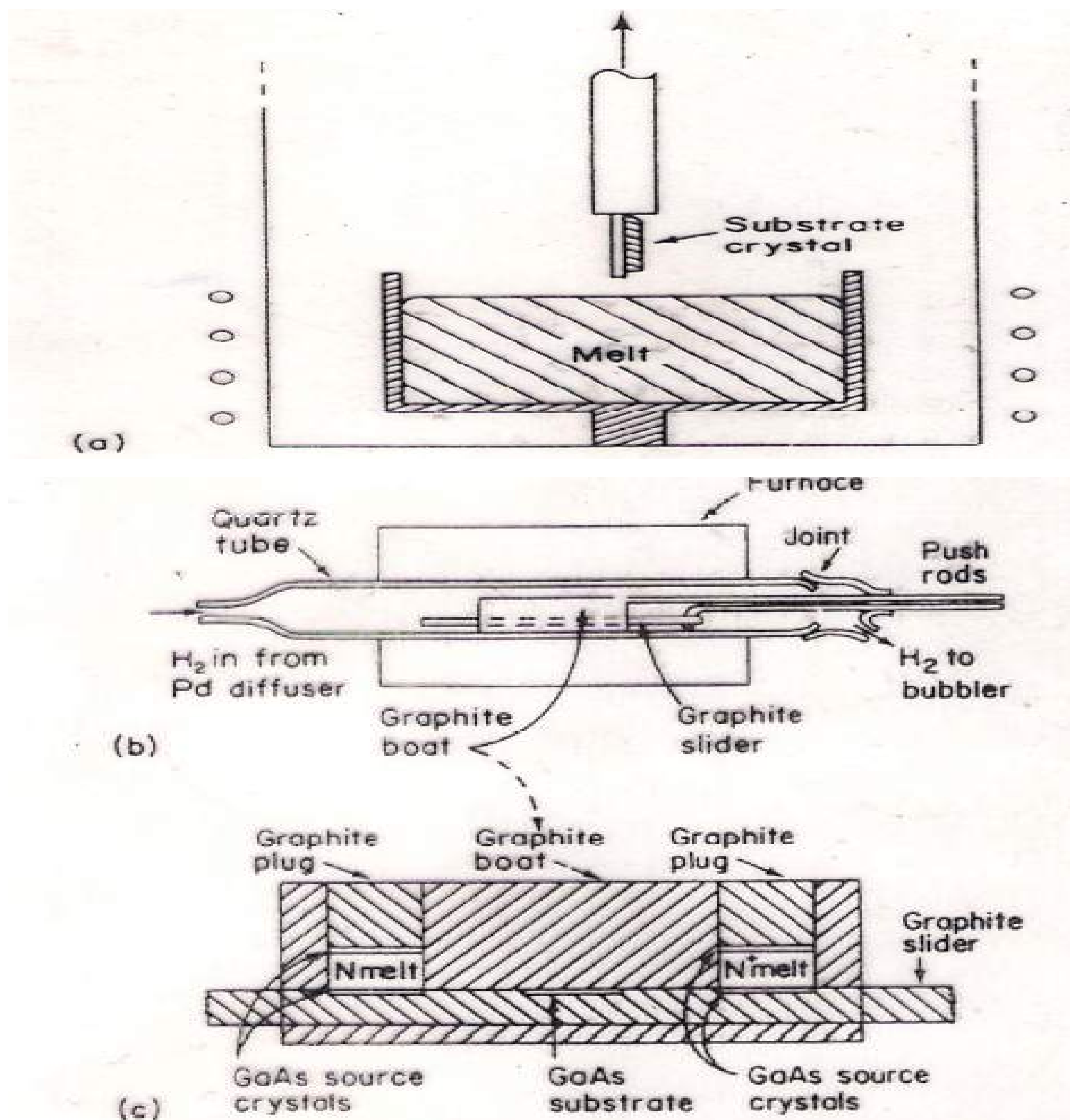


Fig. 2.5 (a) A schematic of the liquid phase epitaxial (LPE) growth system; (b) an LPE system for gallium arsenide; (c) an enlargement of the boat assembly (permission of Cornell University)

Solid state diffusion

In semiconductor technology it is important to control the type and concentration of the impurities with in specific regions of semiconductor crystal practically this is achieved by : (solid state _diffusion)

The electrical characteristics of P-N junctions and other semiconductor devices formed by solid state diffusion can be directly used in the measurement of the impurity concentrations.

Diffusion:

It is the process of introducing selected impurity atoms into designated areas of semiconductors in order to modify the properties of that area.

- The idea was found by Pfann in 1952 to alter the type of conductivity of Si and Ge.
- Diffusion is used to form (bases, emitter and resistors (in bipolar device technology)).
- ((source region ,drain region and doping of polysilicon),(in MOS device technology)).

Dopant atoms can be introduced into Si in many ways :

1. Diffusion from chemical source in vapor form at high temperature.
2. Diffusion from a doped _oxide source.
3. Diffusion and annealing from an ion implanted layer. This provides more precise control of total dopant from 10^{11} to more than 10^{16} Cm^{-2}.it is used to replace the above two methods.

Why studding diffusion ?

1. Attempts to develop improved models from experimental data to predict diffusion results from theoretical analysis.
2. To calculate the electrical characteristics of a semiconductor device from the processing parameters.

Diffusion theories:

Have been developed from two major approaches:

1) The continuum theory of Fick's simple diffusion equation :

Fick's first law : the particle flux density is related to the gradient of the particle density by :

$F = - D * (dN / dx)$ ………………………………………. (1)

Fick's second law: the time rate of change of the particle density is in turn related to the divergence o the particle flux density:

$(dN / dt) = - (df / dx)$ …………………………………………(2)

Combining equqtion (1) and equation (2) gives :

$(dN / dt) = - (df / dx) * (-D *(dN / dx)) = D(d^2N / dx^2)$ ……. …....(3)

Where

D : diffusion constant, N : particle density, f :particle flux density.

2) Atomistic theory: which involves interaction between: point defects, vacancies , interstitial atoms and impurity atoms.

Point defects (imperfections) :

Vacancy : the absence of an atom from a normally occupied site.

Substitution impurity atom: a foreign atom which is in the site of a matrix atom.

Interstitial impurity atom: a foreign atom in an interstice between a matrix atom.

Frankel imperfection: in a crystal, an atom may leave its site, creating a vacancy and dissolve interstitially in the structure the associated vacancy and interstitial atom is called ' Frankel imperfection'.

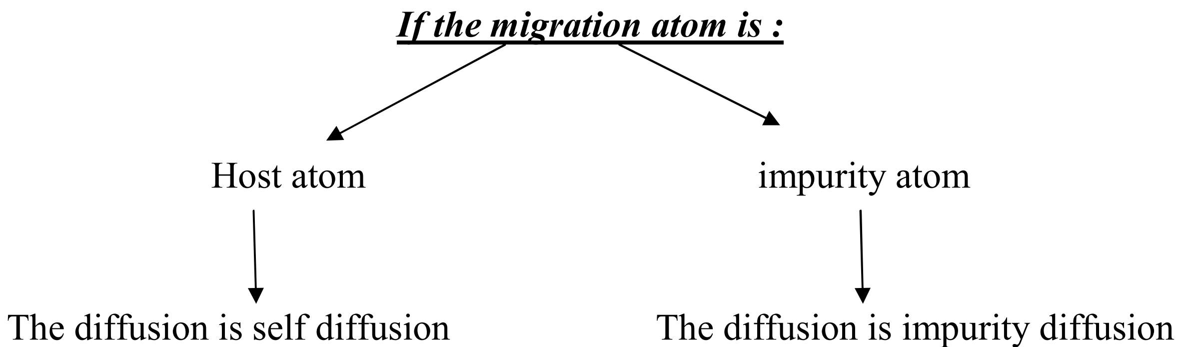
Schottky imperfection: when a cation (+ ve ion) vacancy is associated with an anion (-ve) vacancy, the pair is called (Schottky imperfection).

Model of diffusion in solids :

- At high temperature, point defects such as vacancies and self interstitial atoms are generated in a single crystal solid.
- When a concentration gradient of host and impurity atoms exists, such point defects affects atom movement (diffusion).
- Diffusion in a solid can be visualized as atomic movement of the diffusion in the crystal lattice by vacancies or self interstitials.

Models

1) diffusion by vacancy : sometimes a host atom acquires sufficient energy to leave the lattice site and becoming a self interstitial atom and creating a vacancy, hen neighboring atom (host or impurity) migrate to the vacancy site, it is called diffusion by vacancy.



2)Interstitial diffusion mechanism: an interstitial atom moving from one place to another without occupying a lattice site. An atom smaller than a host atom that does not form covalent bonds with Si often moves interstitially.

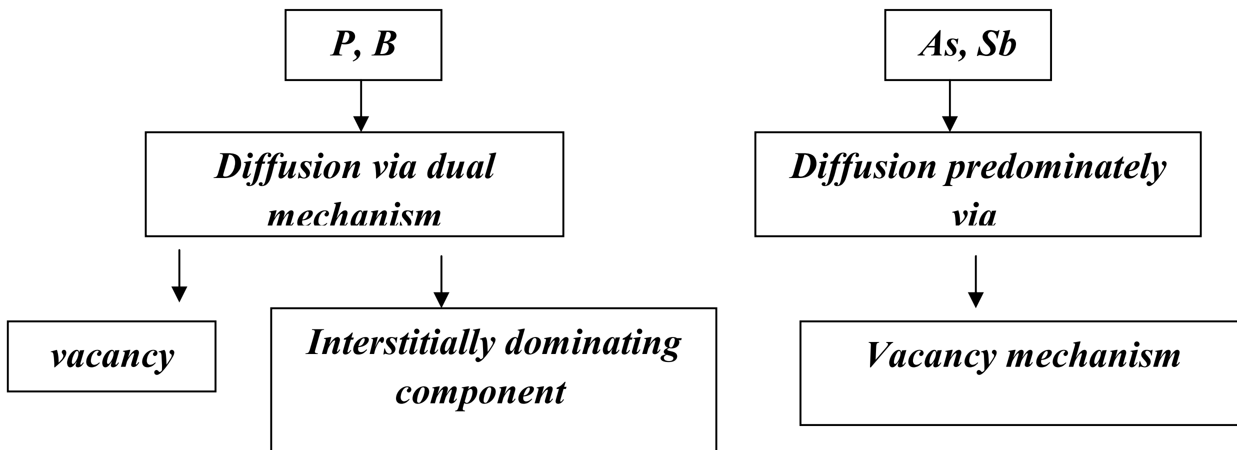
3)Interstitial mechanism (extended interstitial mechanism):

-Atomic movement of self interstitial atom displacing an impurity atom.

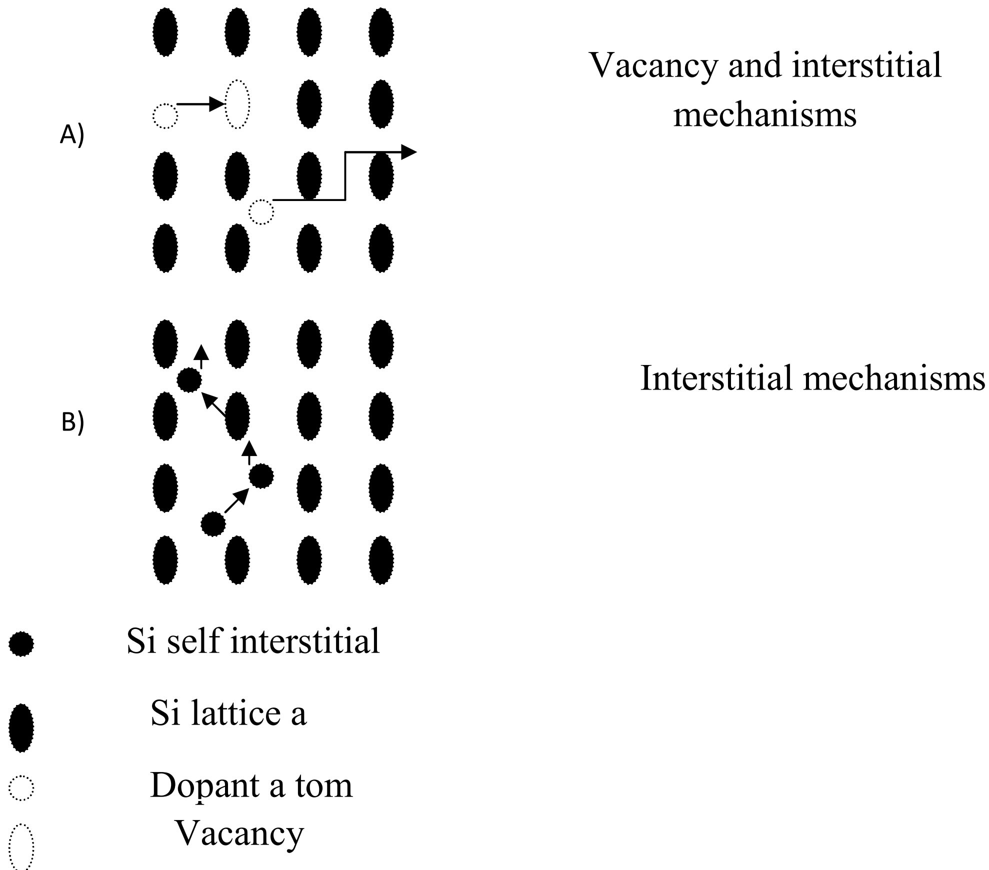
-which is in turn becomes an interstitial atom.

-subsequently, then impurity atom displaces another host atom, and the second host atom becomes a self interstitial.

For dopants :



Models of atomic diffusion mechanism for a two dimension lattice:



Diffusivities of : B, P, As,Sb

-boron, phosphorous, arsenic and sometimes antimony are used as dopant elements for junction formation.

The model of multiple- charge -state point defect –impurity interaction model for diffusion (which is still under development) is used to identify the species contributing to the diffusions

<u>Parameters of which have an effect on the diffusivities :</u>

1. The electric field effect.
2. The band gap _narrowing effect.
3. The high concentration effects.

Substrate doping

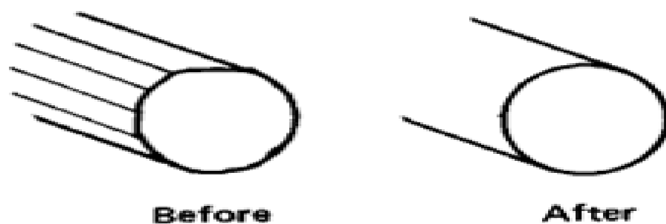
Monolithic integrated circuits are usually fabricated on P – type substrates, so it is necessary to introduce acceptor atoms into the single – crystal silicon at some stage.
A controlled amount of acceptor impurity, often boron, is added to the melt before the crystal is pulled, to produce the required P- type silicon substrate material.
Boron (P- type) doped Czochralski pulled silicon is available in resistivity from (0.0005 to 50 ohm _cm) , Arsenic and phosphorus (n- type) doped silicon crystal is available in resistivity from (0.005 to 40 ohm _cm). Arsenic perfected in the lower resistivity ranges . Antimony is also used 0.01 ohm –cm range. this doping is suitable for growing epitaxial substrates.

4) Ingot slicing to wafers:

After removal from the crystal grower, the crystal goes through a series of steps that result in the finished wafer. First is the cropping off (**End cropping**) of the crystal ends with a saw.

During crystal growth, there is a diameter variation over the length of the crystal Wafer fabrication processing, with its variety of wafer holders and automatic equipment, requires tight diameter control to minimize warped and broken wafers.

Diameter grinding is a mechanical operation performed in a center less grinder. This machine grinds the crystal to the correct diameter without the necessity of clamping it into a lathe-type grinder with a fixed center point—although lathe-type grinders are used.



Crystal Diameter Grinding

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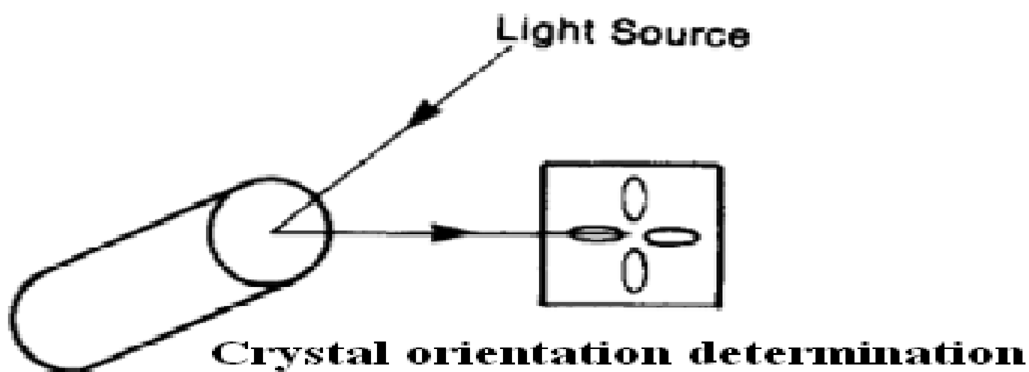
Before the crystal is submitted to the wafer preparation steps, it is necessary to determine whether it meets orientation and resistivity specifications. The crystal orientation is determined by either X-ray diffraction or collimated light refraction. In both methods, an end of the crystal is etched or polished to remove saw damage. Next, the crystal is mounted in the refraction apparatus and the X-rays or collimated

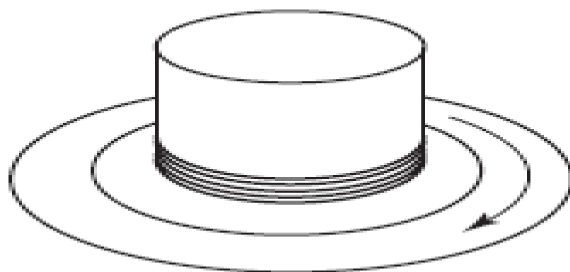
light reflected off the crystal surface onto a photographic plate (X-rays) or screen (collimated light). The pattern formed on the plate or screen is indicative of the crystal plane (orientation) of the grown crystal. The pattern shown in Figure below is representative of a 100 orientation. Most crystals are purposely grown several degrees off the major 111 or 100 plane. This off-orientation provides several benefits in wafer fabrication processing, particularly ion implantation.



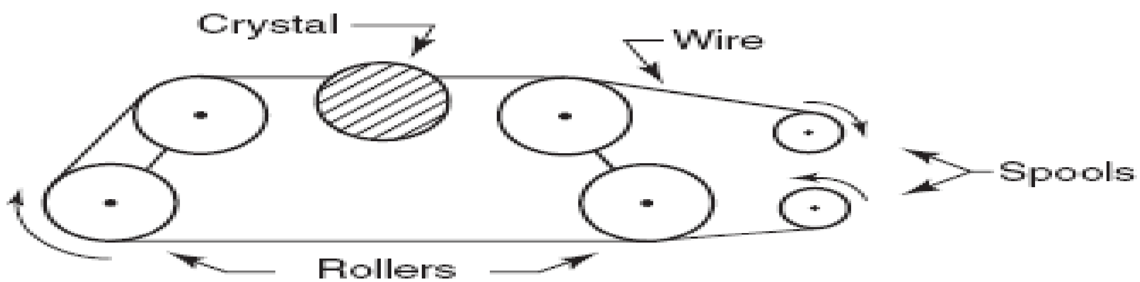
Crystal orientation determination

The crystal is positioned on a slicing block to ensure that the wafers will be cut from the crystal in the correct orientation. Because each crystal is doped, an important electrical check is the conductivity type (N or P) to ensure that the right dopant type was used. A hot-point probe connected to a polarity meter is used to generate holes or electrons (depending on the type) in the crystal. The conductivity type is displayed on the meter. The amount of dopant put into the crystal is determined by a resistivity measurement using a four-point probe .The resistivity is checked along the axis of the crystal due to dopant variation during the growing process. This variation results in wafers that fall into several resistivity specification ranges. Later in the process, the wafers will be grouped by resistivity range to meet customer specifications. Then, the

wafers are sliced from the crystal with the use of diamond-coated inside diameter saws (Figure below) These saws are thin circular sheets of steel with a hole cut out of the center. The inside of the hole is the cutting edge and is coated with diamonds. An inside diameter saw has rigidity, but without being very thick. These factors reduce the ***kerf (cutting width***) size which in turn prevents sizable amounts of the crystal being wasted by the slicing process. For 300-mm diameter wafers, wire saws are used to ensure flat surfaces with little tapering and with a minimal amount of "kerf" loss.



a. Inside Diameter Diamond Saw



b. Wire Saw

Figure 3.19 Inside-diameter saw wafer slicing.

<u>*)Wafers etching and polishing:*</u>

These slices which as cut ,are quite rough, are then lapped to remove saw marks and to produce a flat surface . surface damage, which after this operation can still exist to around 20μm ,is removed with a chemical etch employing an acid mixture consisting of nitric acid to oxidize the surface and hydrofluoric acid to dissolve the oxide.

The slices are then polished mechanically on a wheel to a mirror_ like finish, using alumina abrasive powders of decreasing grit size down to a final 1μm diameter .surface damage, which is still present down to around 2μm deep, is finally removed by an additional chemical etching stage, which can sometimes be simultaneous with the final polishing stage.

6) Batch processing of requires circuits:

The main process steps are:

Oxidation

Can be defined as the process by which a layer of (SiO_2) is formed on the surface of (Si).

Oxidation processes :

1- Vapor Phase Reaction (CVD).
2- Plasma anodisation .
3- Wet anodisation.
4- Thermal oxidation (in both dry and wet environment).

Application of oxide layer in IC technology

1- Provide surface passivation for (Si) devices.
2- Serve as a diffusion mask.
3- Isolate one device from another.
4- Isolate the gate electrode from the Si in FET devices.
5- Isolate multiple levels of devices interconnected in IC circuits.

There are two aspects to understanding the oxidation of (Si) :

1- Understanding oxidation technologies to grow oxides which are suitable for IC circuit applications.
2- Interaction between device characteristics and the electrical and chemical properties of the oxide layer can affect device characteristics it has (3) effect on electrical properties of Si in IC circuit technology there are:

A- Oxidation_ induced stacking faults (as which are structural defects at Si surface because they can be electrically active causing increased junction leakage and reduced minority carrier injection efficiency.

B- Redistribution of ionized impurities at Si surface which can alter the I/V characteristics and C/V characteristic of MOS devices.

C- Strain in the oxide and in the Si.

Pre oxidation preparation :

1- Saw.
2- Chemically etch.
3- Polish.
4- Cleaning.

Etching processes :

1 -Chemically etching:

There are many chemical etches such as :

For Si :

a) Hydrofluoric acid (HF).
b) Mixture of (HF) and (NH_4F).
c) HF :HNO_3 :CH_3COOH 3:5:3
d) HF :HNO_3 1:3
e) NaOH or KOH

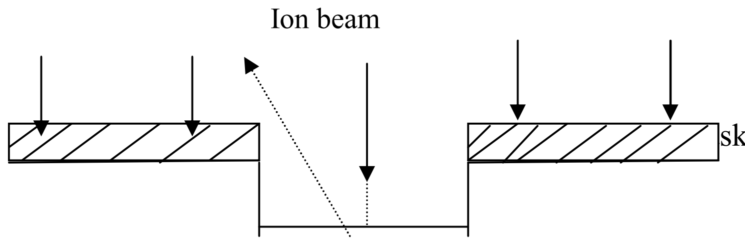
FOR GaAs:

a) (1-20 %) Br_2 in ch3cooh.
b) HF :HNO_3 :H_2O 1:3:2
c) H_2SO_4 :H_2O_2 :H_2O 3:1:1

2.Plasma etching

3.ion beam etching (ion milling):

1. *Incident ion*
2. *Sputtered atom*



(ion milling)

Pre cleaning procedure :

1- Degreasing :by trichloroethylene and acetone.
2- Removing organic contaminants :by exposure wafer to boiling mixture of :
   - distilled water.
   - ammonium hydroxide.
   - hydrogen peroxide.
3- Metallic impurities removal : by a mixture HCl, hydrogen per oxide and distilled water.
4- Removing the oxide which is performed during cleaning :by dillet solution of hydrofluoric acid and de – ionized water.

Thermal growth

It is the process of the film formation on a large variety of substrates by heating them in gas of required type :

Oxygen : for oxides.

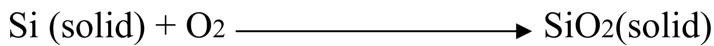
Nitrogen : for nitrides

CO : for carbides.

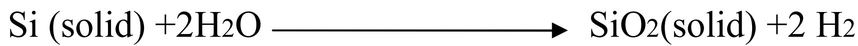
Thermal oxidation

SiO_2 layrs on Si prepared by different methods such as :

1- Vapor phase reaction.
2- Electrochemical oxidation (anodization).
3- Plasma reaction.
4- Thermal oxidation through chemical reaction.

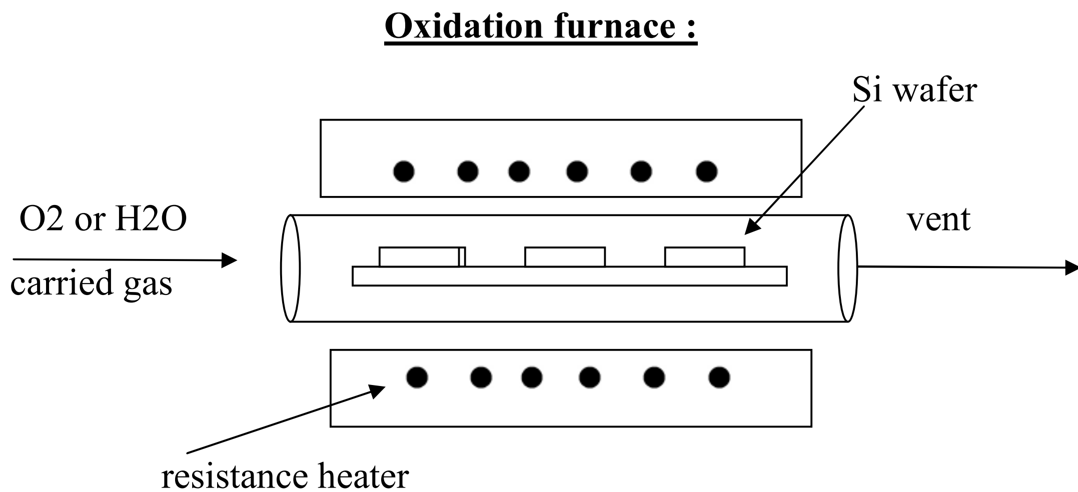


Si (solid) + O_2 ⟶ SiO_2(solid)



Si (solid) +2H_2O ⟶ SiO_2(solid) +2 H_2

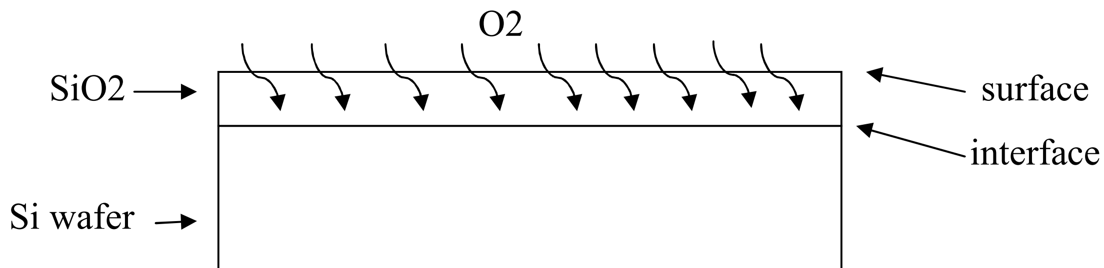
Oxidation furnace :



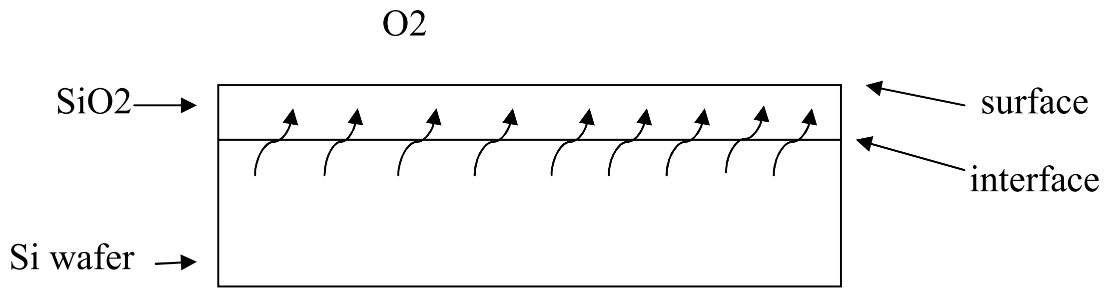
higher temperature will increase the thickness obtained in a given time because the mobility of both substrate and oxygen ions increase with temperature.

Possible ways in which SiO2 films may be formed :

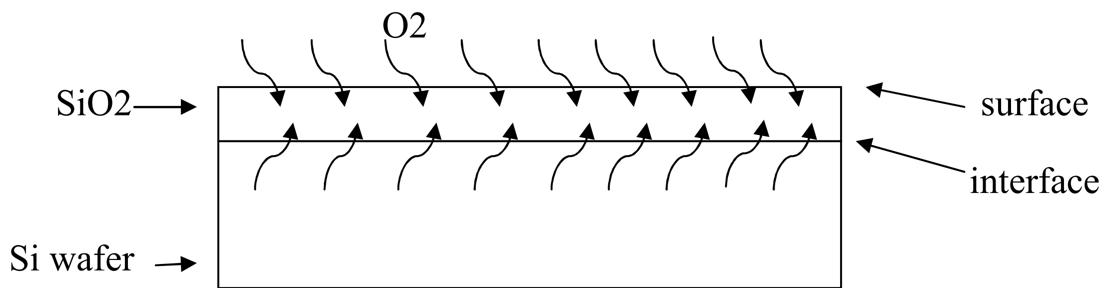
- ❖ O2 moves through film and SiO2 formed at interface.



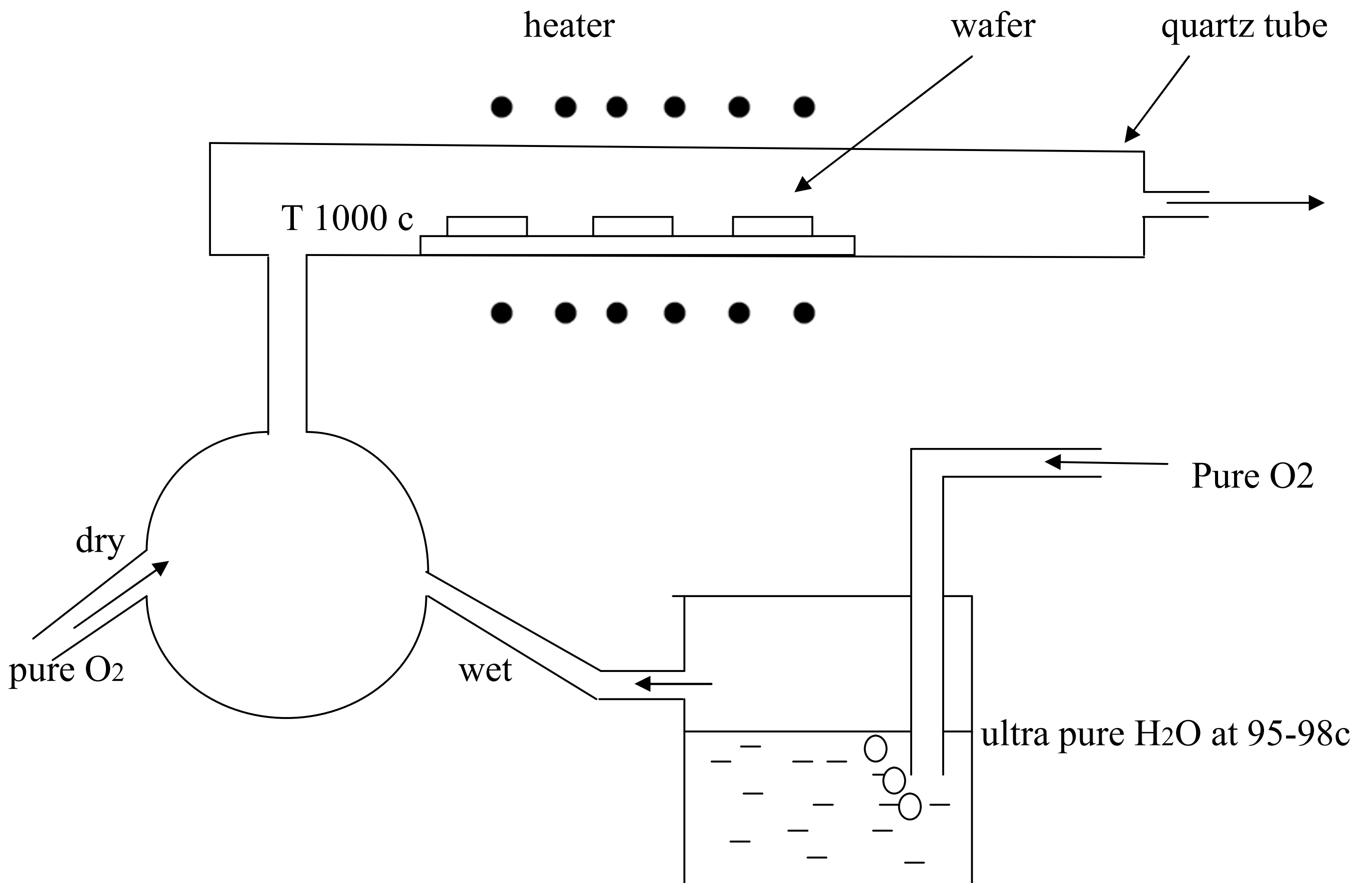
- Si moves through film and SiO_2 formed at surface.



- O_2 and Si moves into film and SiO_2 formed within oxide layer.



Thermal oxidation system



an analysis yield the following relationship between film thickness (Xo) and time (t):

$$Xo = \frac{A}{2} \left[\sqrt{\left(1 + \frac{t+\tau 0}{\frac{A^2}{4B}}\right)} \quad -1 \right]$$

Where A, B are constants for agiven type of oxide at agiven temperature.

0 : is a correction factor (for dry oxides).

$$\tau 0 = \frac{Xi^2 + AXi}{B}$$

where Xi is initial value of oxide thickness.

$$A = K1\ e^{\frac{E1}{KT}}$$

$$B = K2\ e^{\frac{-E2}{KT}}$$

$$K = \text{Boltzmann constant} = \frac{1.38\ 10^{-23}}{1.6\ 10^{-19}} = 8.63 * 10^{-5}\ eVK^{-1}$$

EXAMPLE : a dry thermal oxide 0.2 Mm thick is required to be gron at 1100 C^oon (111) orientation silicon .calculate the time required ?

Solution:

T (in Kelvin) = 1100+273= 1373

KT = 8.63 *10^{-5} *1373 = 0.119 eV

From table , we get :

K1=1.24 *10^{-4} Mm , K2=772 $Mm^2/_{hr}$ E1 = 0.77 eV

E2 = 1.23 eV Xi =0.02 Mm

$$A = 1.24 * 10^{-4} \; e^{\frac{0.77}{0.119}} = 0.08 \text{ Mm}$$

$$B = 772 \; e^{\frac{-1.23}{0.119}} = 0.025 \; \text{Mm}^2/_{hr}$$

$$0 = \frac{(0.02)^2 + 0.08 \quad 0.02}{0.025} = 0.082 \text{ hr}$$

$$Xo = \frac{A}{2} \left[\sqrt{\left(1 + \frac{t + \tau 0}{\frac{A^2}{4\,B}}\right)} - 1 \right]$$

$$0.2\text{Mm} = \frac{0.08 \text{ Mm}}{2} \left[\sqrt{\left(1 + \frac{t + 0.082 \text{ hr}}{\frac{(0.08)^2 \; \text{Mm}^2}{4 \; (0.025) \; \text{Mm}^2/_{hr}}}\right)} - 1 \right]$$

$$0.4 / 0.08 = \left[\sqrt{\left(1 + \frac{t + 0.082 \text{ hr}}{0.064 \text{ hr}}\right)} - 1 \right]$$

$$5 = \sqrt{\left(1 + \frac{t + 0.082 \text{ hr}}{0.064 \text{ hr}}\right)} - 1$$

$$6 = \sqrt{\left(1 + \frac{t + 0.082 \text{ hr}}{0.064 \text{ hr}}\right)}$$

$$36 = 1 + \frac{t + 0.082 \text{ hr}}{0.064 \text{ hr}}$$

$$35 = \frac{t + 0.082 \text{ hr}}{0.064 \text{ hr}}$$

$$35 * 0.064 \text{ hr} = t + 0.082 \text{ hr}$$

$$t = 2.158 \text{ hr}$$

Note : what happen if you repeat the above example for temperature = 800 C^0 (Impractical).

Example / an oxide is grown for 130 minutes at 1100 C^0 on (100) silicon by passing oxygen through a(95 C^0) water path. Calculate the resulting oxide thickness.

Example / an oxide is grown for 1 hour at 950 C^0 on (100) silicon by

- Dry oxygen
- Steam grown oxide.

Calculate the resulting thicknesses and comment.

Example / compare the time taken to grow a 1Mm silicon oxide film at 1100 C^0 using:

- Dry oxygen
- Steam grown oxide

Numerical values of parameters for oxidation processing

parameter	(111) silicon			(100) silicon		
	wet	**pyrolytic**	**dry**	**wet**	**pyrolytic**	**dry**
K1 *Mm*	**2.3 $*10^{-6}$**	**2.37 $*10^{-6}$**	**1.24 $*10^{-4}$**	**4.02 $*10^{-6}$**	**3.98 $*10^{-6}$**	**2.08 $*10^{-4}$**
K2 Mm^2/hr	**214**	**386**	**772**	**214**	**386**	**772**
E1 eV	**1.29**	**1.27**	**0.77**	**1.29**	**1.27**	**0.77**
E2 eV	**0.71**	**0.78**	**1.23**	**0.71**	**0.78**	**1.23**

Xi *Mm*	**0**	**0**	**0.02**	**0**	**0**	**0.02**

Lithography

It is the technique generally used in the semiconductor industry for all pattern formation.

Lithography types are (photolithography, electron beam, X-ray)

Technique requirements :

1- It must be suitable for forming patterns in different types of surface film.
2- It is necessary to be able to (align) each pattern level accurately with the preceding one.
3- The dimensional accuracy of each individual pattern must be sufficient to ensure proper alignment between levels.
4- The chip size or repeat distance must be accurately maintained between different levels since any error would accumulate across the array and lead to misrigistration on some circuits within the array.

Similarity between photolithography and photography:

1- Light –sensitive film, or emulsion.
2- Controlled exposure to an image.
3- Development process.

Photolithography process:

1- The Si wafer is first oxidized.

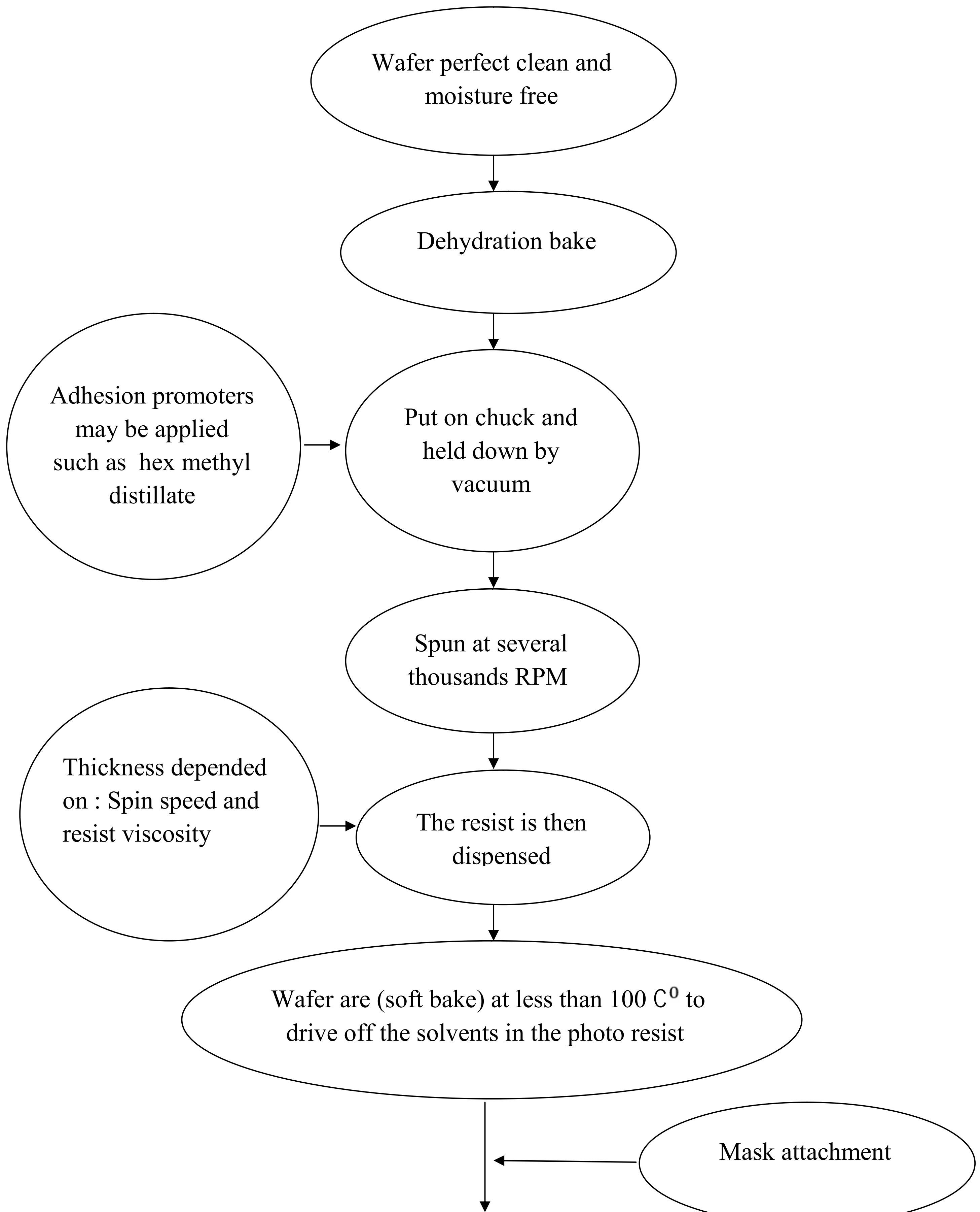
2- The wafer is coated with U.V light sensitive film. (negative photo resist consist of (base of synthetic rubber compounds few% of light sensitive agent)).the exposed area remain, while the unexposed are removed).
3- A glass mask containing the pattern of the appropriate level is brought into contact with the wafer.
4- The whole is then expose for the correct exposure time to a collimated beam of U.V light, following which the mask is removed.
5- The resist film on the wafer is then removed.
6- A suitable etch has to be used which will remove SiO2 but not attack the photo resist film or the under lying Si significantly. When the SiO2 in the uncovered areas and the photo resist has been removed, we have achieved the final objective of producing pattern (windows) in the SiO2 ready for diffusion.

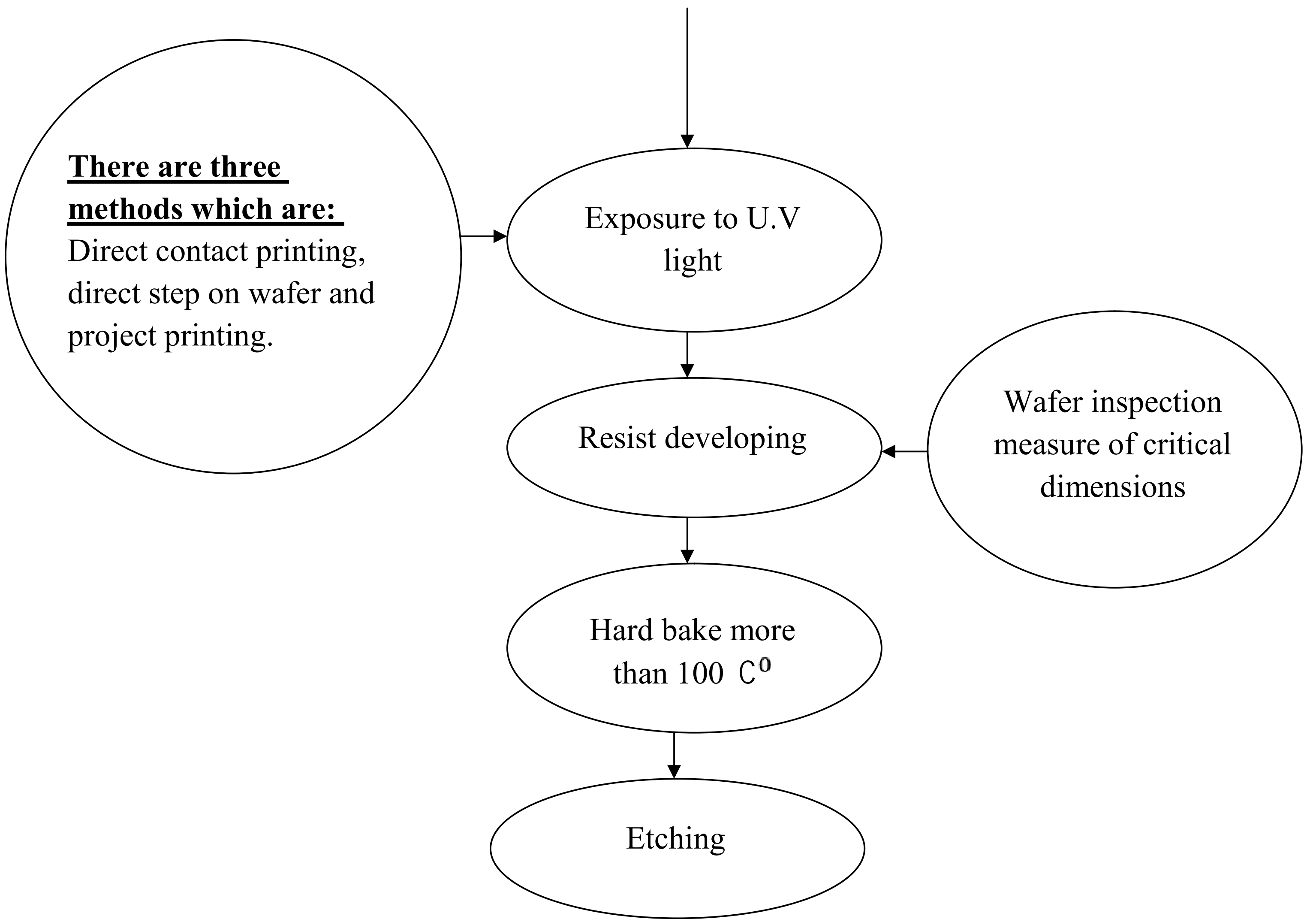
- ***Instead of exposing photo resist through a mask, an electron beam can be used to write directly on the wafer***
- ***Such E-Beam pattern generators evolved from scanning electron microscopes.***
- ***This exposure is accomplished either by:***

*1- **raster scan :** where the beam is fixed in position and wafer moves in an XY raster scanning motion.*

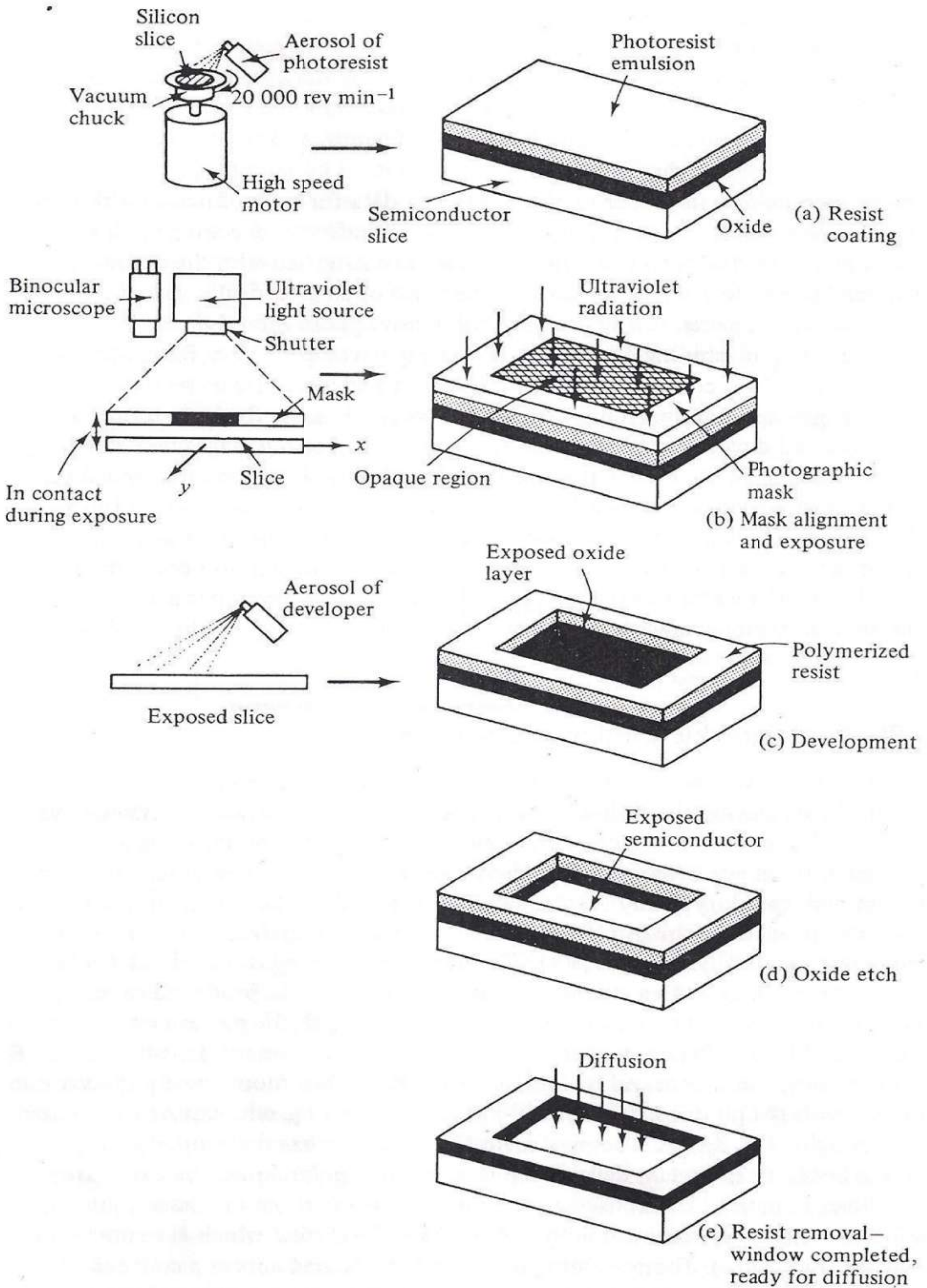
2- Vector scan : *where the wafer is fixed and beam is moves.*

Photolithography process





There are three methods which are:
Direct contact printing, direct step on wafer and project printing.
Exposure to U.V light
Resist developing
Wafer inspection measure of critical dimensions
Hard bake more than 100 C°
Etching



Preparation of windows in the oxide layer for the location of diffusions into a silicon slice.

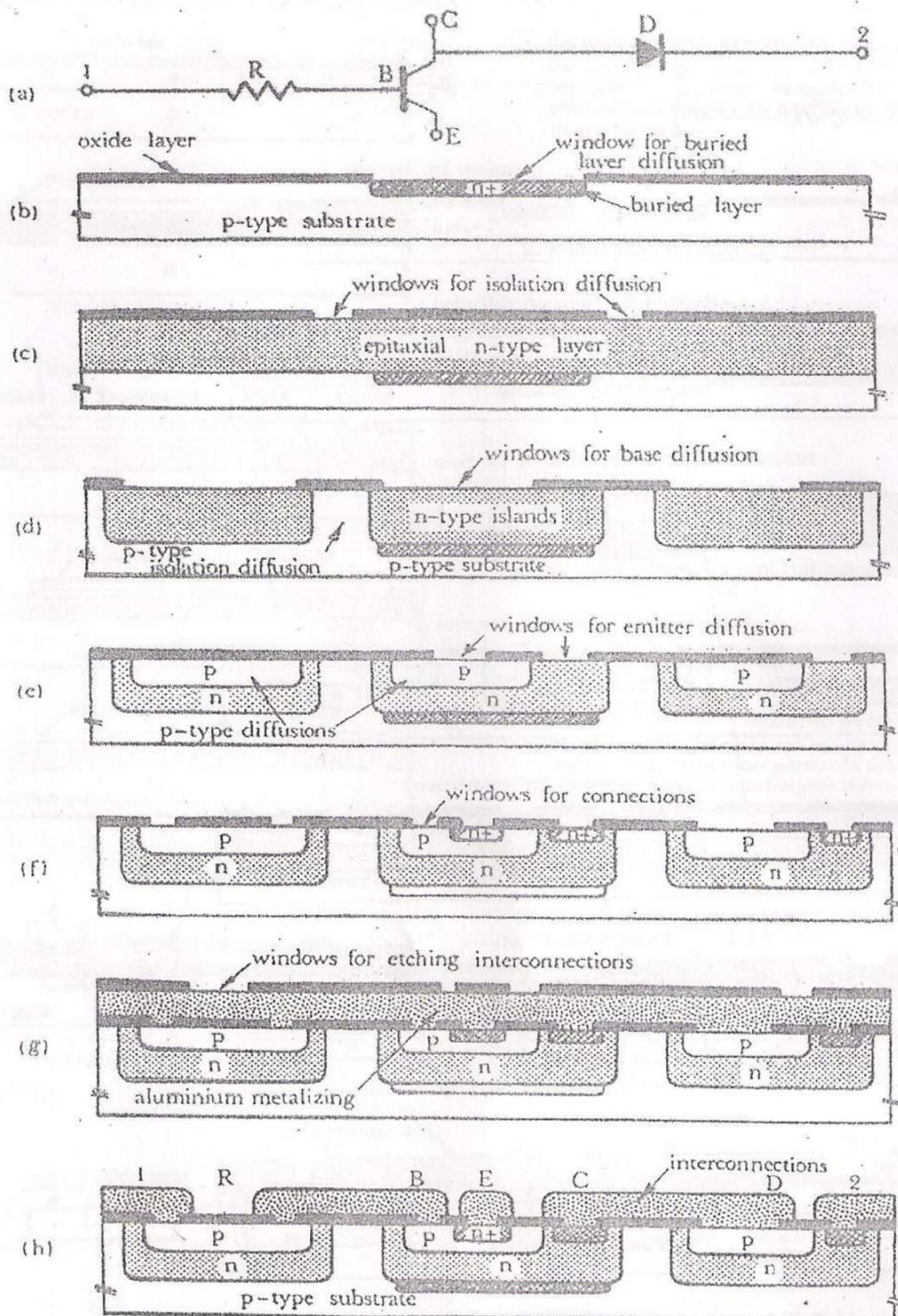


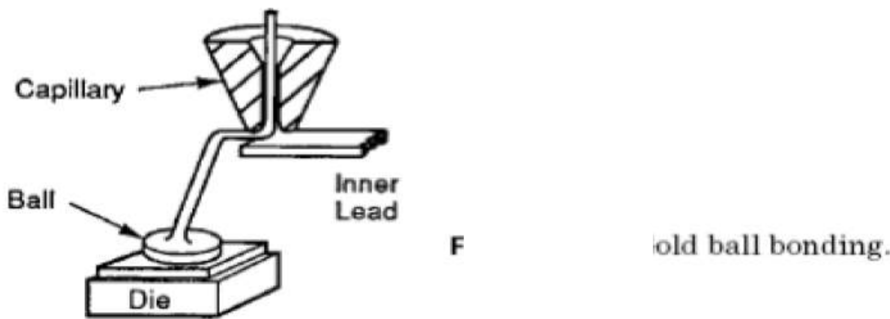
Fig. 13.9 Fabrication of a monolithic integrated circuit.

7) *Wafer slicing to chips (die)* :

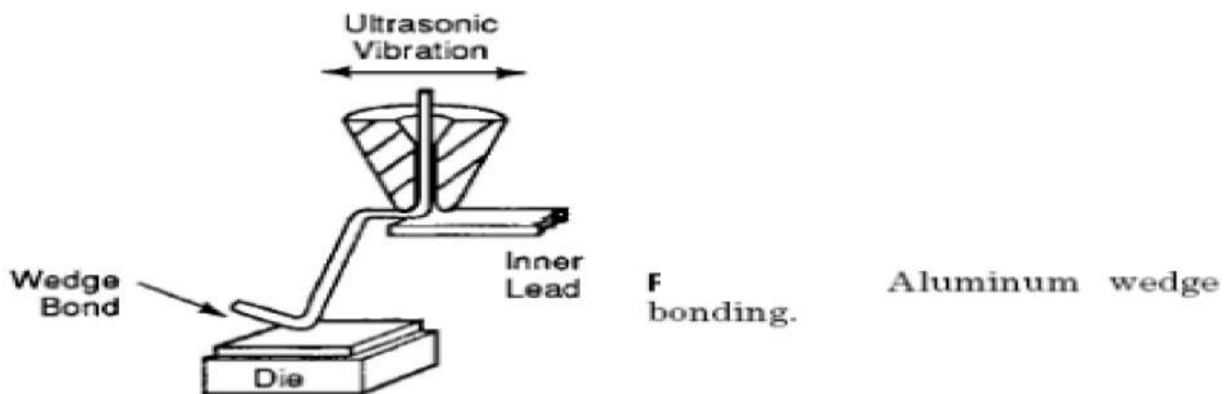
There are many methods to wafer slicing to chips like diamond saw and laser beam induced holes.

8) *Die mounting, Wire bonding and Hermetic* :

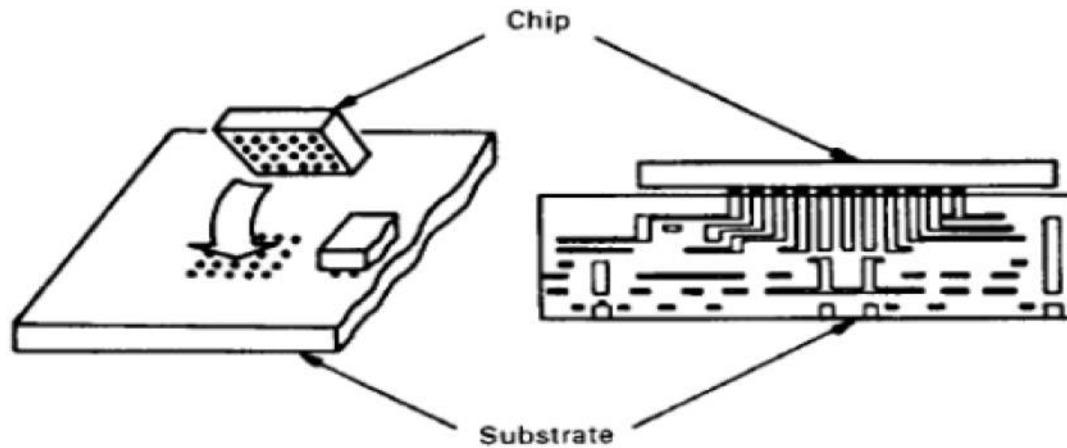
Before the die are encapsulated, they are mounted on to lead frames, and thin gold wires connect the bonding pads on the chip to the frames to create the electrical path between the die and lead fingers. There are method to get wire bonding like (heating, Ultrasonic wedge bonding and flip chip beam lead bonding) Product samples are taken out of the normal product flow for environmental and reliability assurance testing.



F old ball bonding.

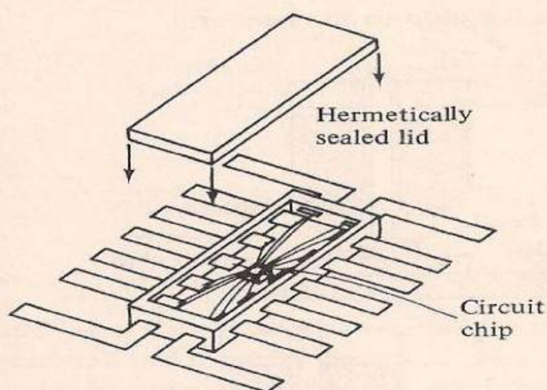


F Aluminum wedge bonding.

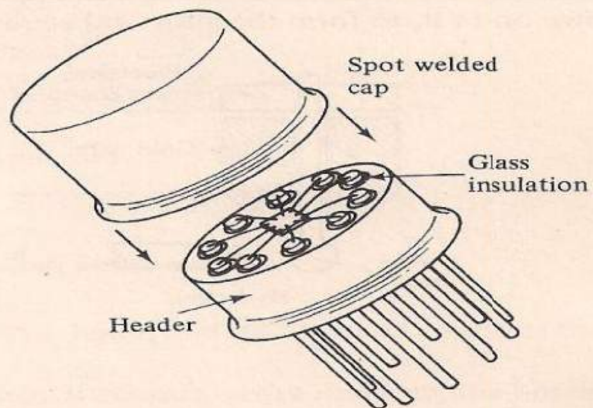


F.___ ___ Flip-chip joining. *(Source:* Microelectronics Handbook, *by Tummala and Rymaszewski.)*

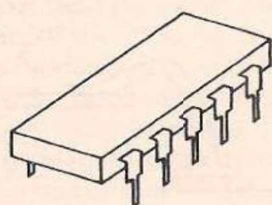
These quality assurance test push chips to their extreme limits of performance to ensure high quality, reliable die and to assist engineering with product and process improvements. During Encapsulation, lead frames are placed onto mold plates and heated. Molten plastic material is pressed around each die to form its individual package. The mold is opened, and the lead frames are pressed out and cleaned.

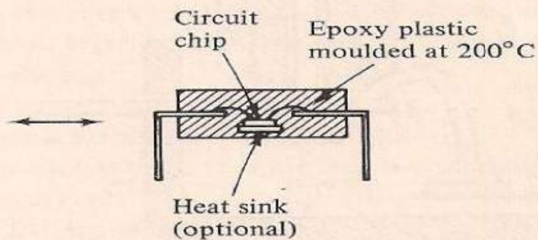


(a) Flat pack



(b) Transistor pack





(c) Dual-in-line package

Fig. 6.9 Integrated circuit packages.